ISSCC 2016

SESSION 6

Image Sensors

Panasonic

An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e- Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor

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Masashi Murakami, Yasunori Inoue

Panasonic Corporation, Japan

Outline

- Background
- Organic-Photoconductive-Film (OPF) CMOS Image Sensor
- Simultaneous-Capture Wide-Dynamic-Range
  - Dual-Sensitivity Pixel
- Reset Noise Cancellation
  - Capacitive-Coupled Noise Canceller
- Characterization Results
- Using MIM Capacitor
- Conclusion

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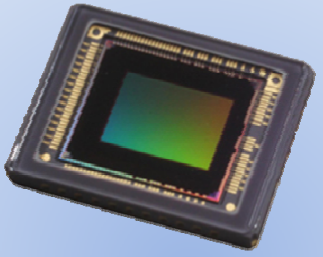
Image Sensors become “Key Devices”

In-vehicle



“Key Devices”

Medical

Mobile

Surveillance

Broadcast

DSL

Robot vision

- **Needs for “Imaging” and “Sensing”**
- **Wide Dynamic Range (High Saturation/Low Noise)**
- **High Sensitivity**
- **High Frame Rate**

…

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Image Sensors Performances

OPF: Organic Photoconductive Film
WDR: Wide Dynamic Range

	Common Si Sensor	WDR Si Sensor	VLSI 2013 OPF Sensor	This Work
High Sensitivity	X1.0	X1.0	**X1.2**	→
Range of Incident Light	30degrees	30degrees	**60degrees**	→
Simultaneous -Capture DR	76dB	100dB	**88dB**	↗

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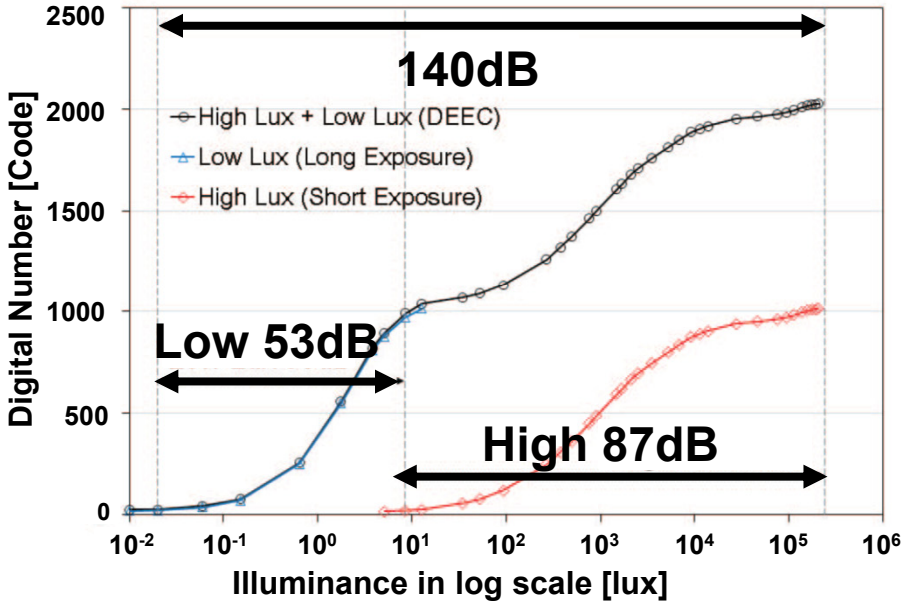
Conventional WDR Methods

- **Synthesizing multiple exposures lead to asynchronous problem.**

A. Y. Chiou VLSI2015

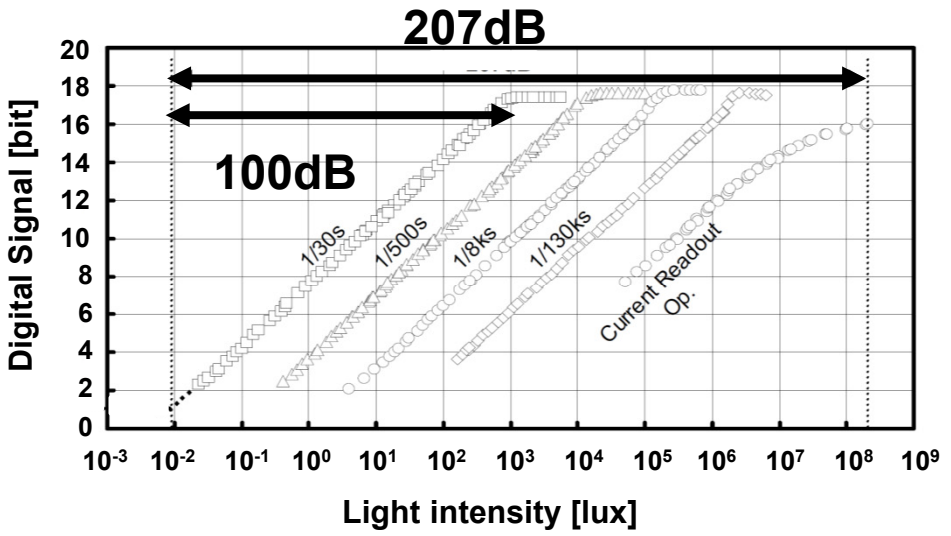
Multiple exposures in a frame



DR using exposure time:140dB
Simultaneous-capture DR:87dB

N. Akahane ISSCC2006

Lateral overflow integration capacitor



DR using exposure time :207dB
Simultaneous-capture DR:100dB

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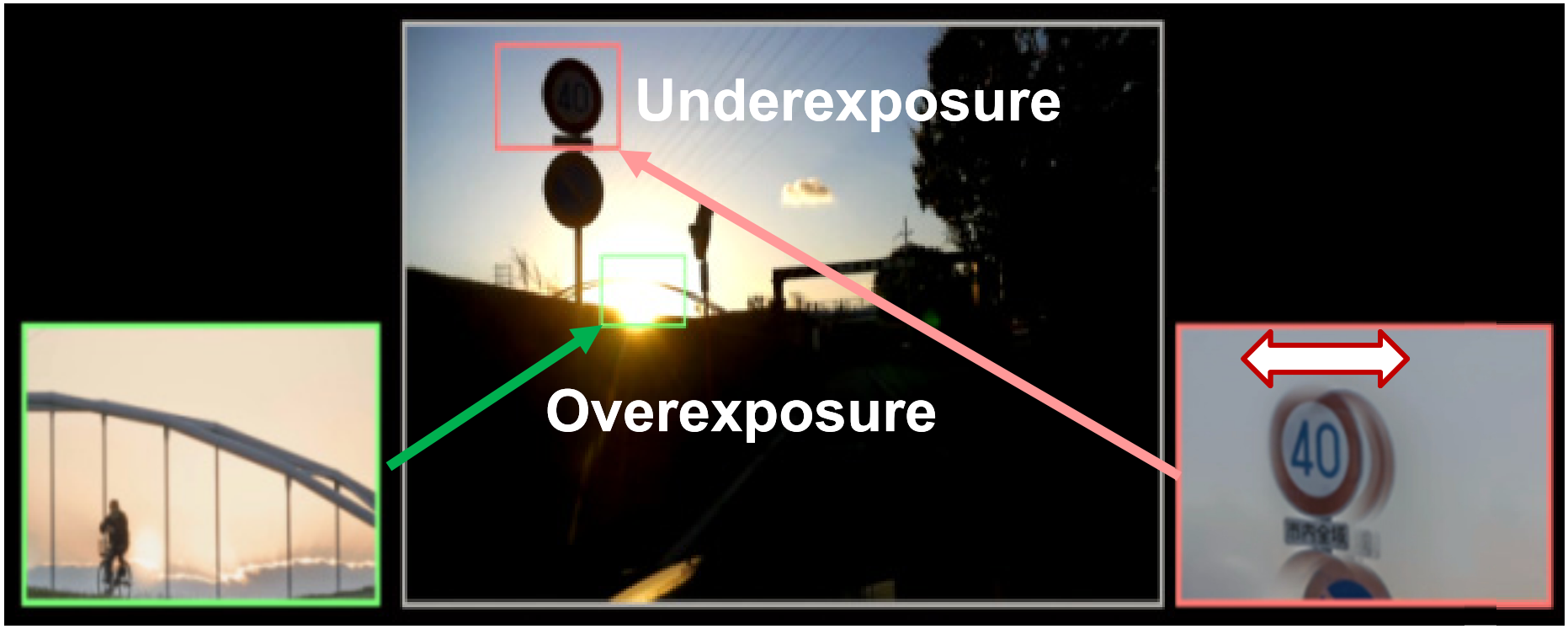
Motion Blur Problem

- Preventing motion blur is important



Motion blur
at high-speed imaging

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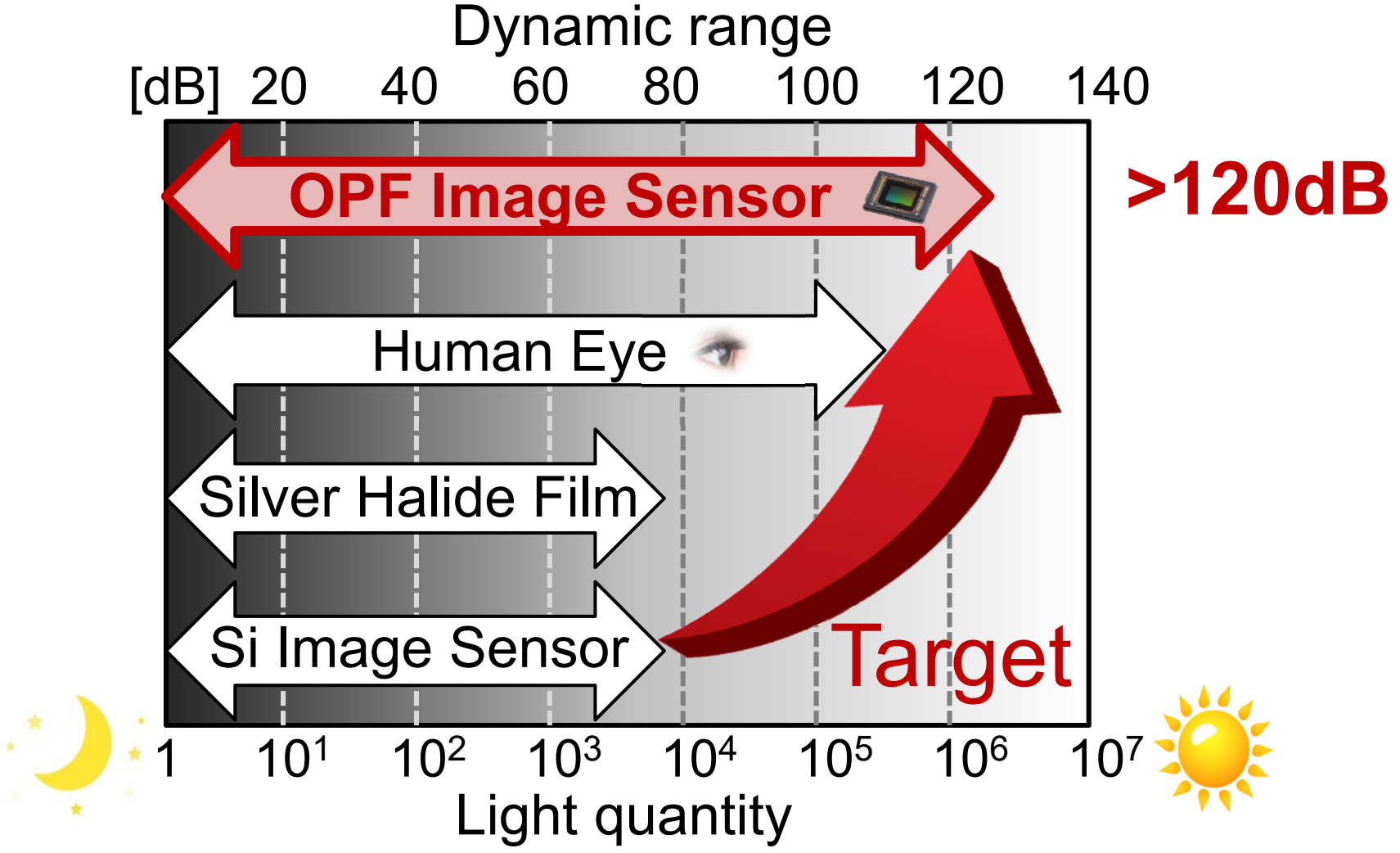
SCWDR Target

SCWDR: Simultaneous-Capture Wide Dynamic Range

- **To exceed the human eye's capacity**



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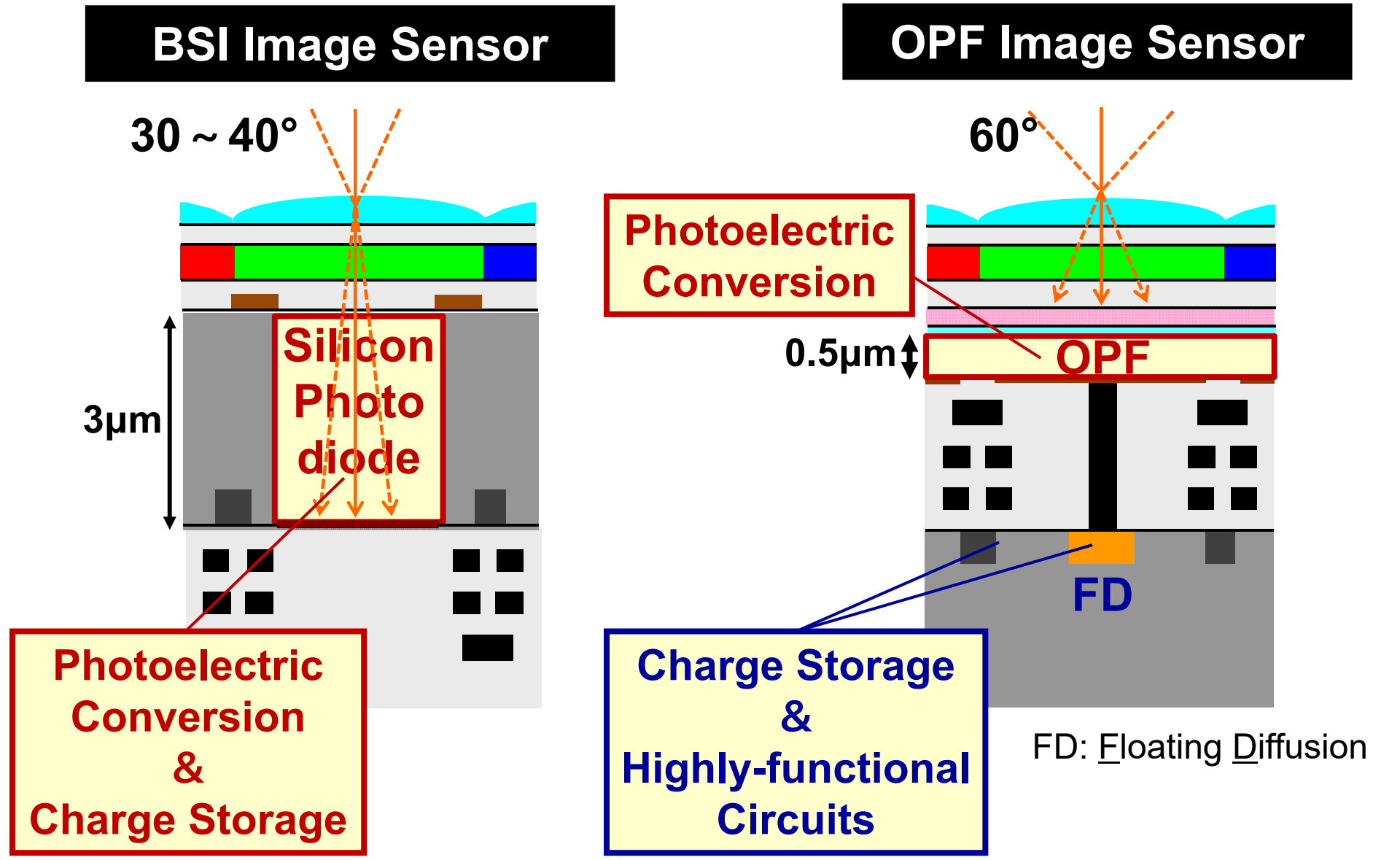
OPF Image Sensor



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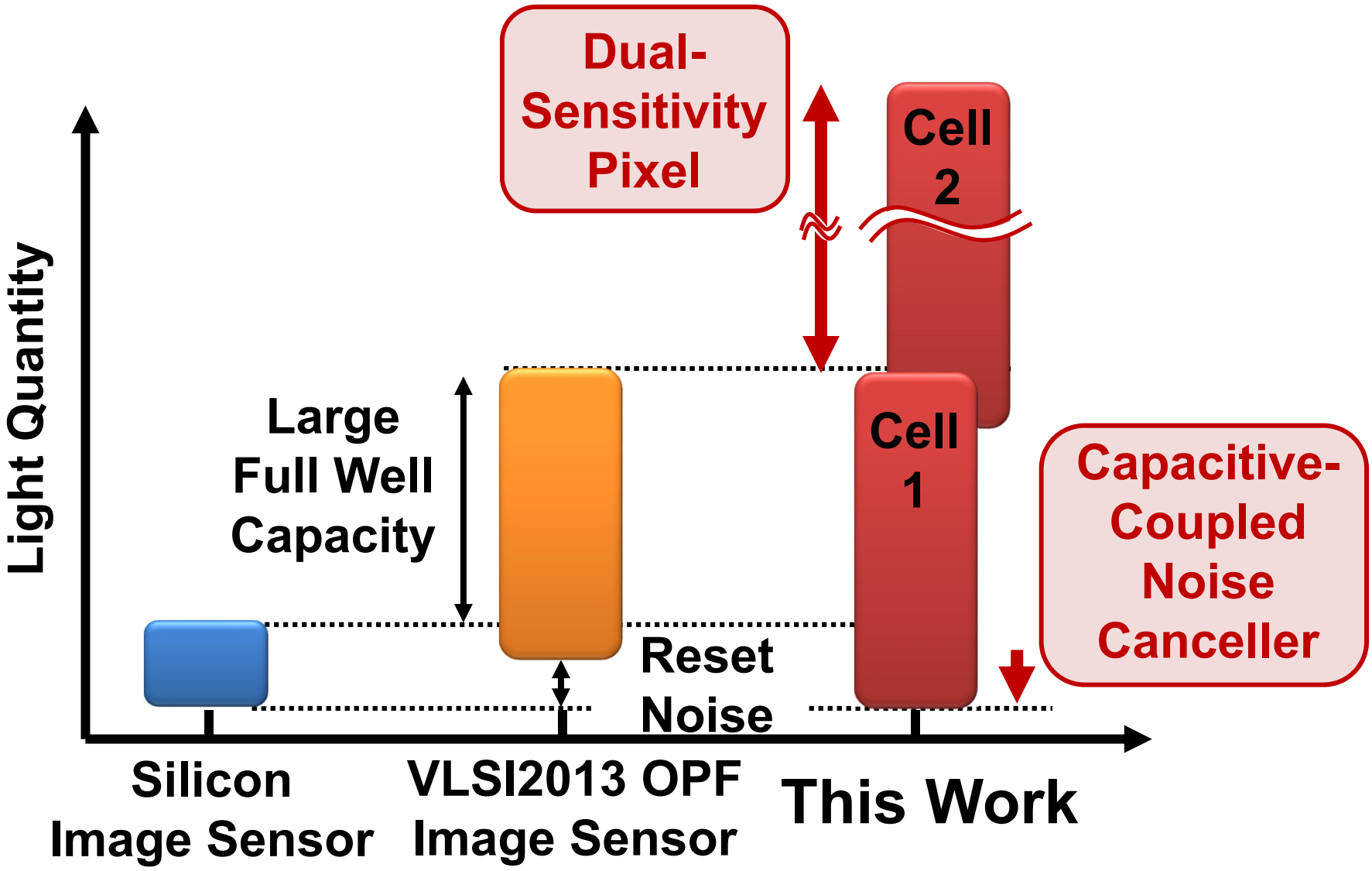
Our Wide Dynamic Range Techniques



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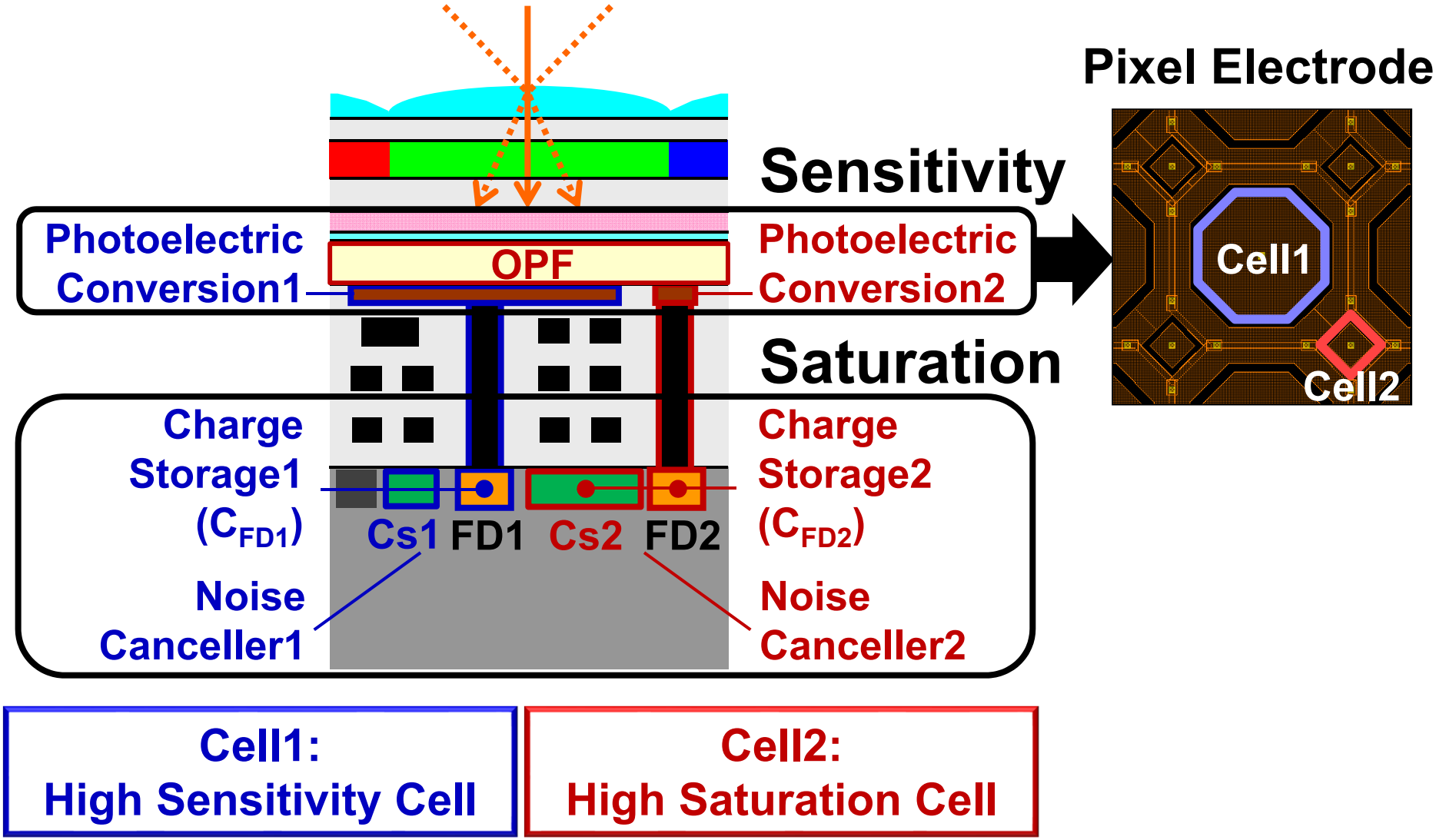
Dual-Sensitivity Pixel (DS-Pixel)

One "DS-Pixel"



Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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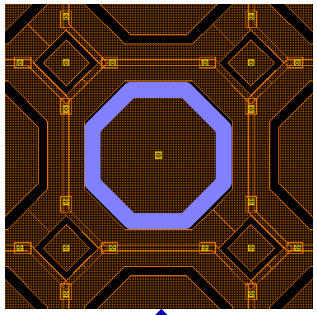
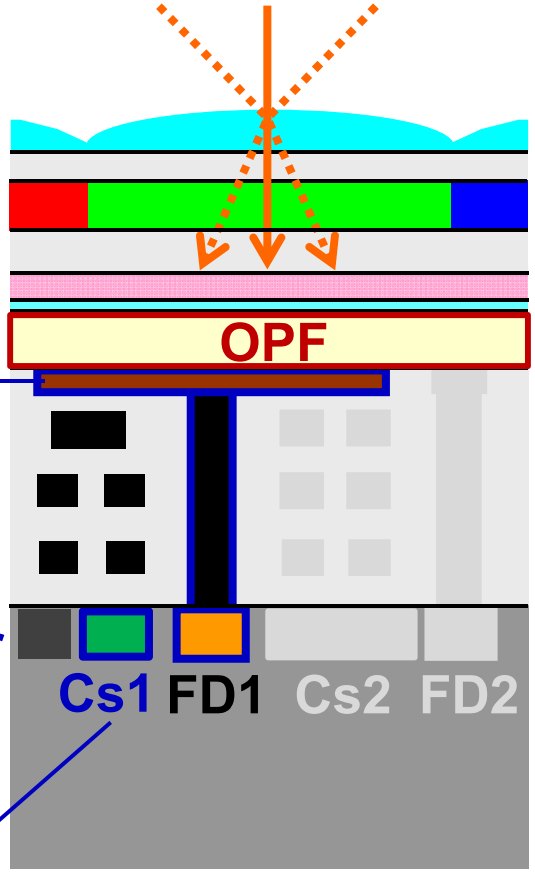
Cell1: High Sensitivity Cell



High Sensitivity Electrode

One "DS-Pixel"



Small Charge-Storage Capacitor

New Noise Canceller

Important

- High Sensitivity
- Low Noise

Not important

- High Saturation

Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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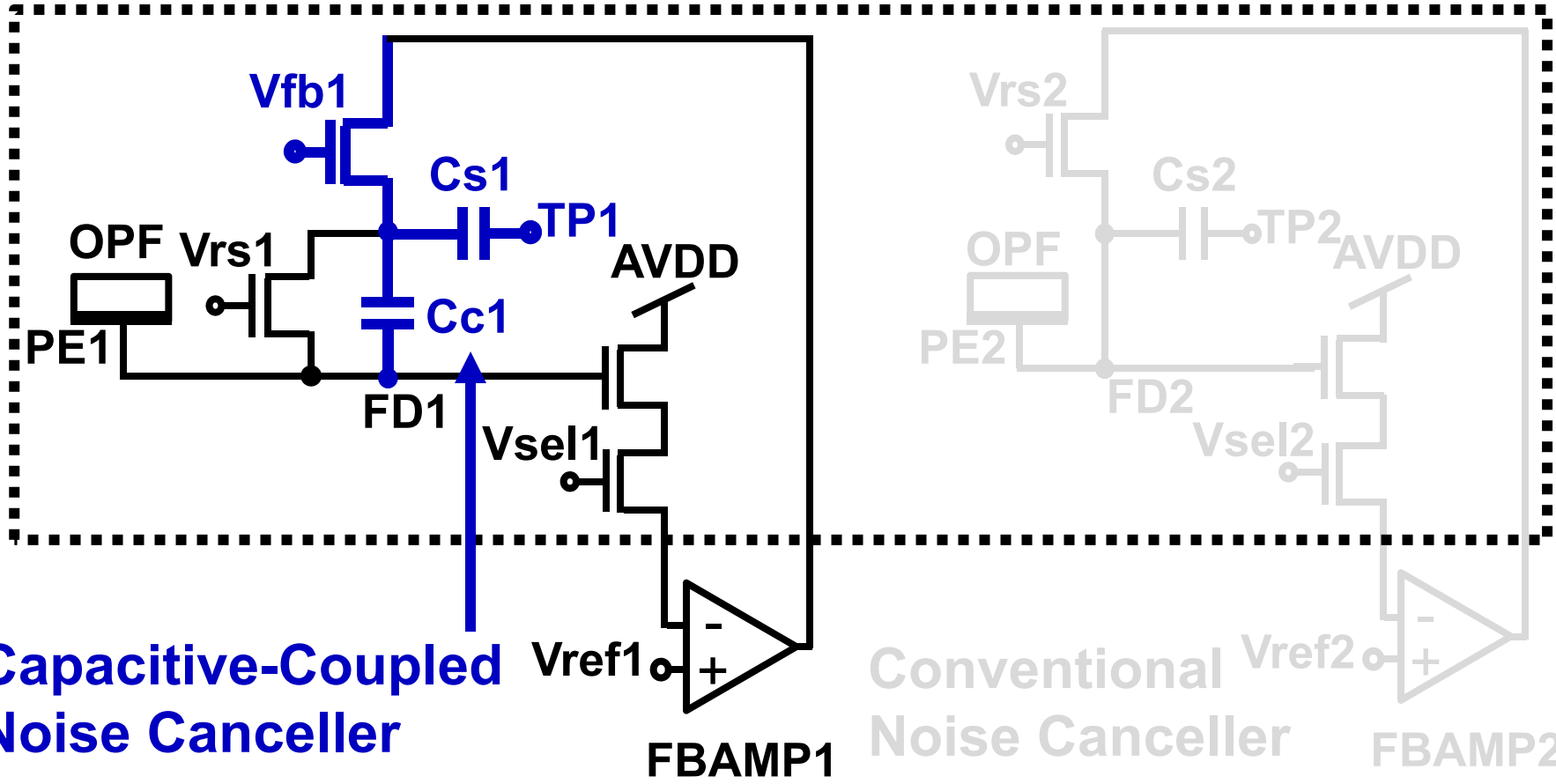
Cell1: High Sensitivity Cell

One “DS-Pixel”



Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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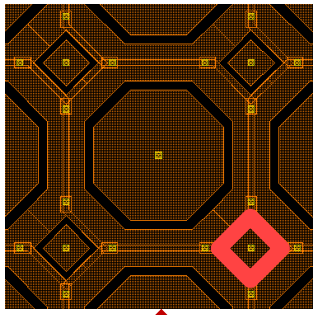
Cell2: High Saturation Cell

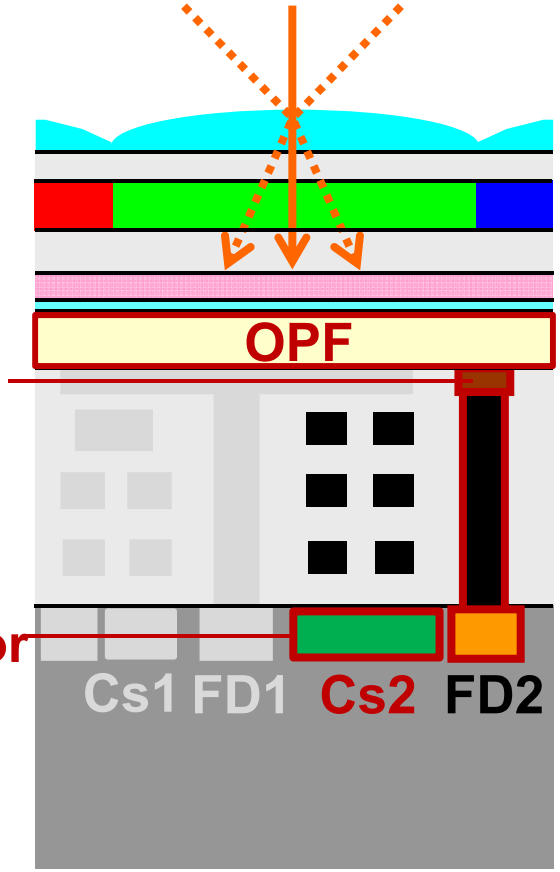


Low Sensitivity Electrode

Large Charge-Storage Capacitor

Conventional Noise Canceller

One "DS-Pixel"



Important

- High Saturation

Not important

- Low Noise

(buried in shot noise)

Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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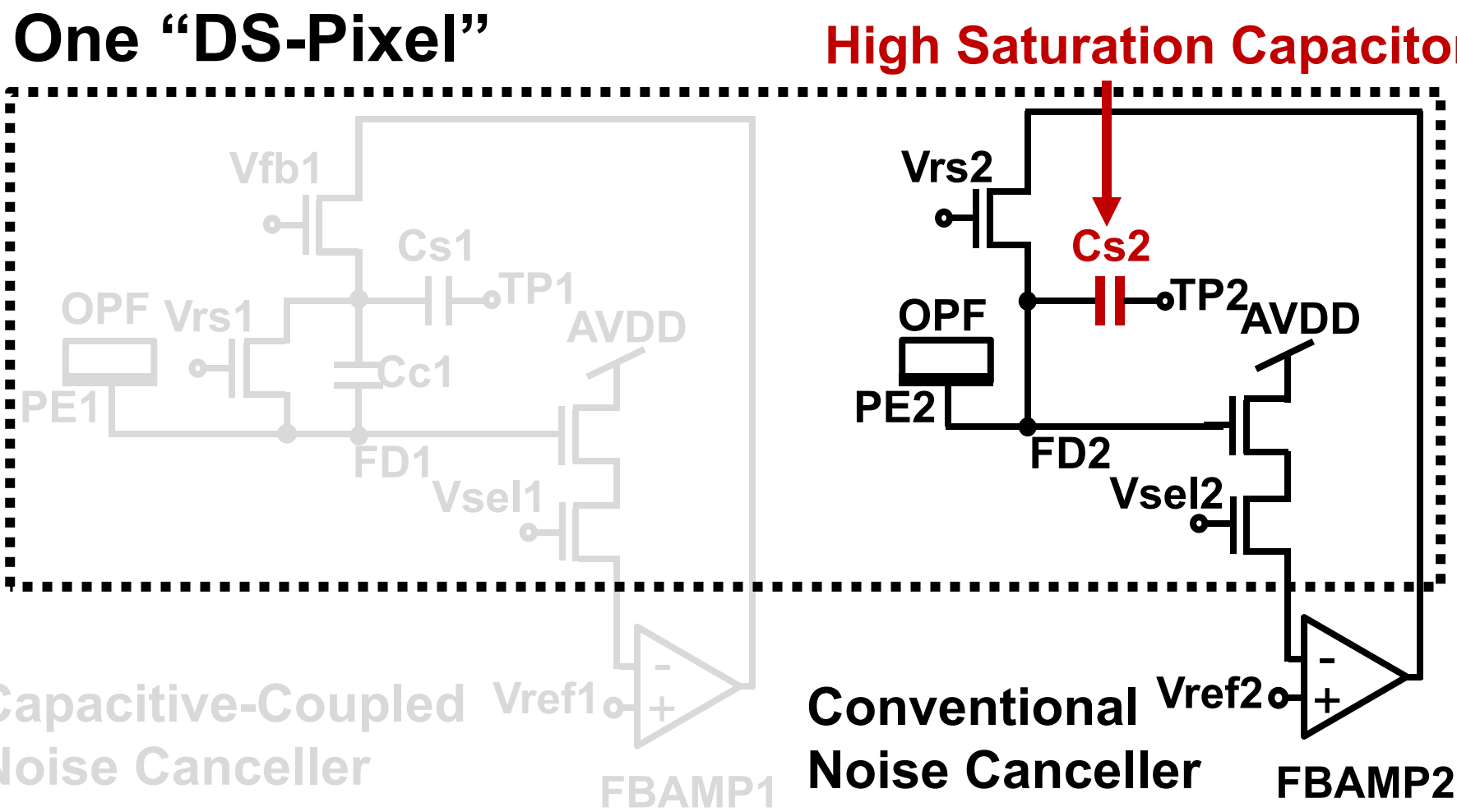
Cell2: High Saturation Cell



Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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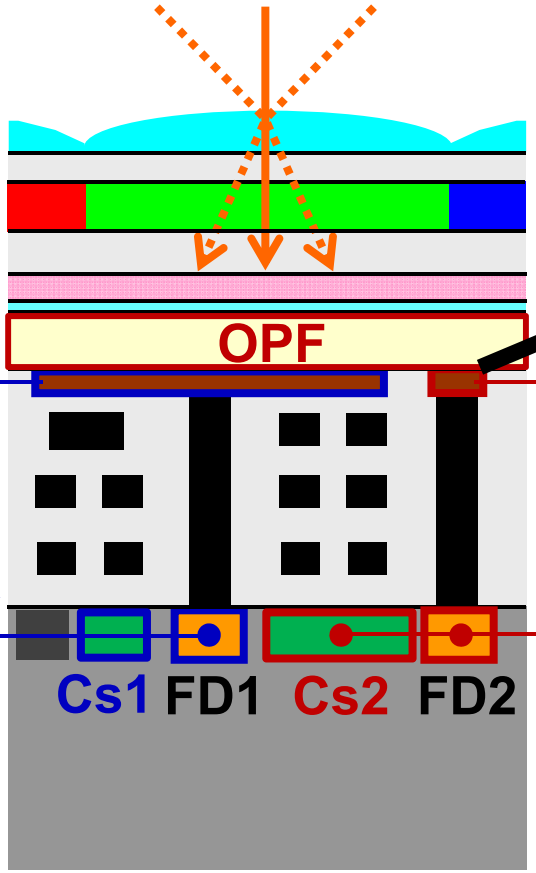
The Effect of "DS-Pixel"

One "DS-Pixel"



High Sensitivity Electrode (PE1)

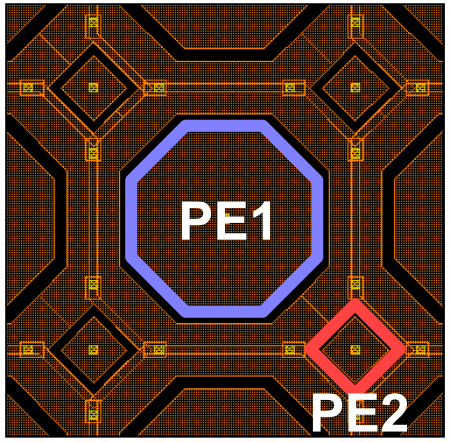
Small Charge-Storage Capacitor (C_{FD1})

Low Sensitivity Electrode (PE2)

Large Charge-Storage Capacitor (C_{FD2})

$C_{FD1}:C_{FD2}=1:10$

Pixel Electrode



$PE1:PE2=1:\frac{1}{10}$

100 times SCWDR

SCWDR: Simultaneous-Capture Wide Dynamic Range

Cell1: High Sensitivity Cell

Cell2: High Saturation Cell

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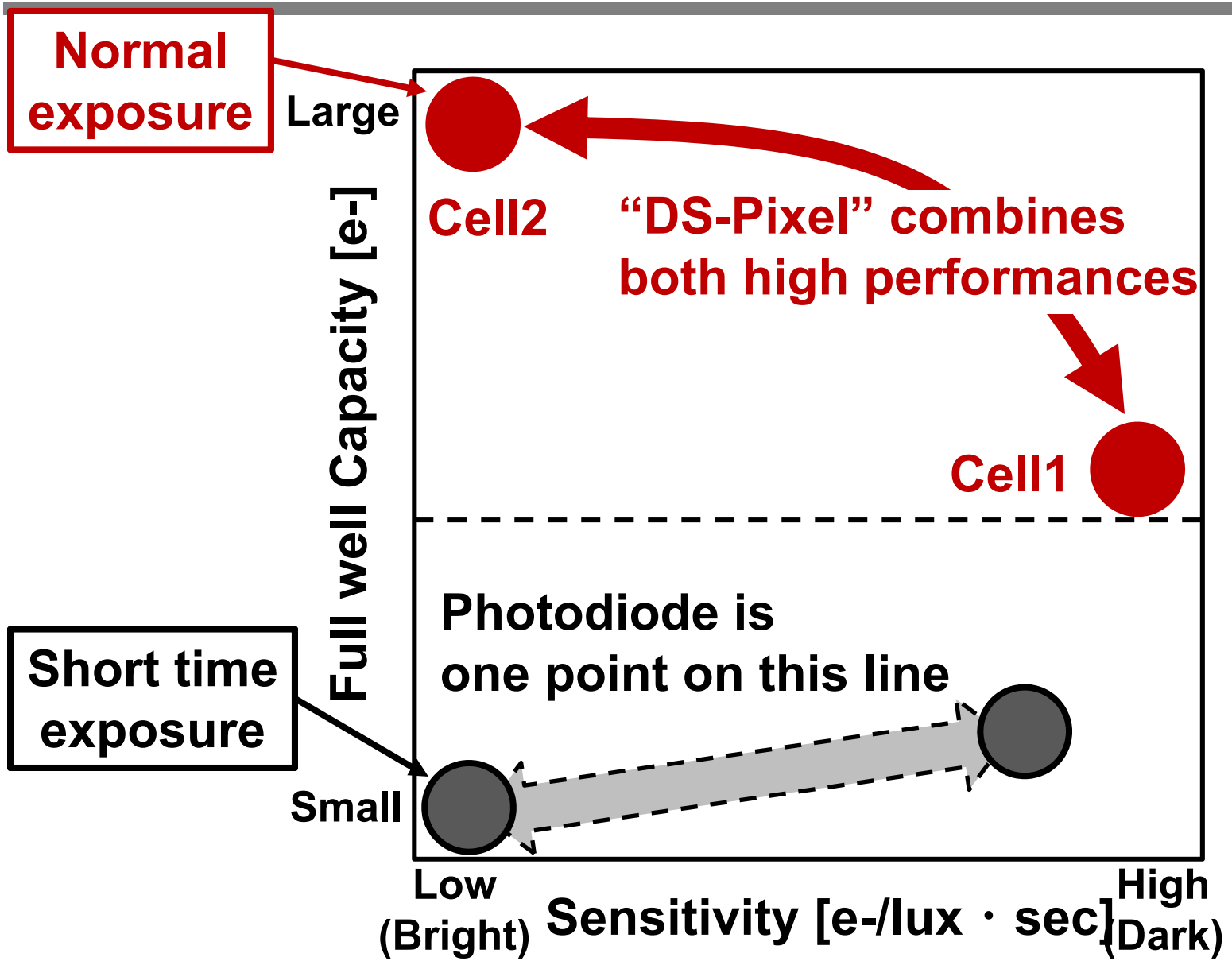
“DS-Pixel ”Performances



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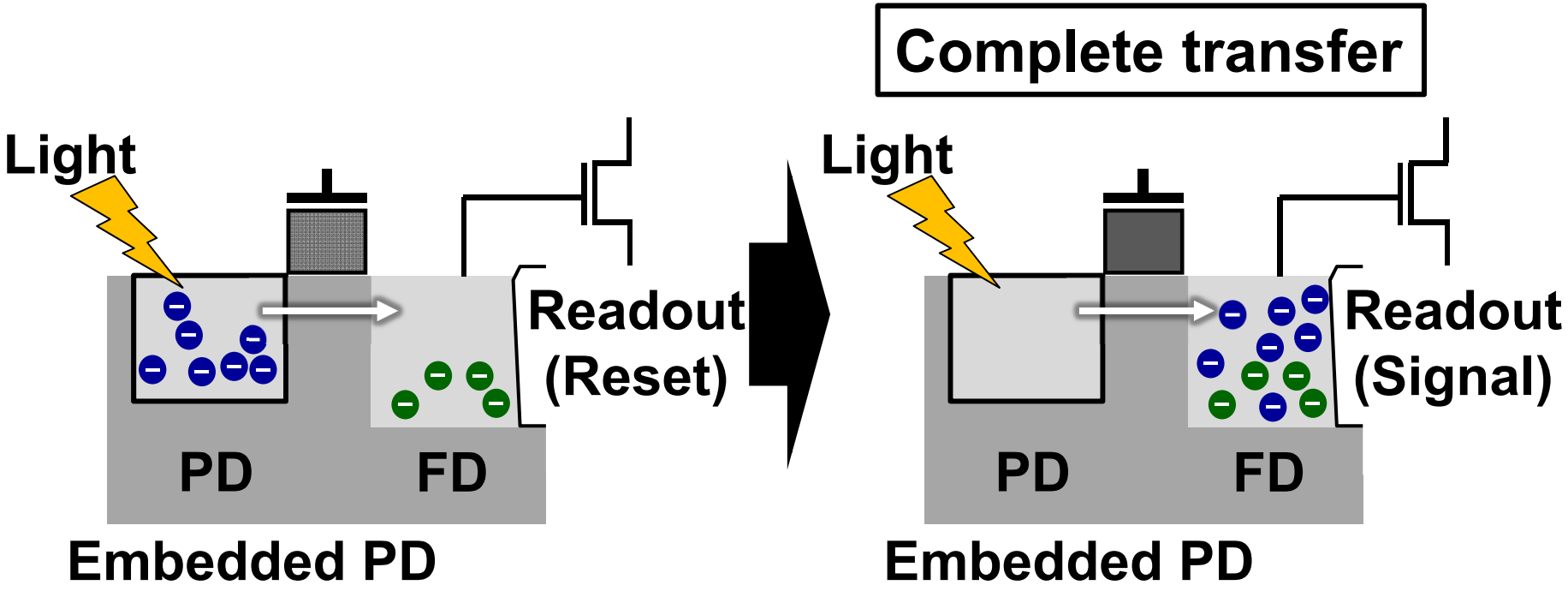
Reset Noise in Dark Region

Silicon Image Sensor



CDS method can be used
Reset noise is not a problem

CDS: Correlated Double Sampling

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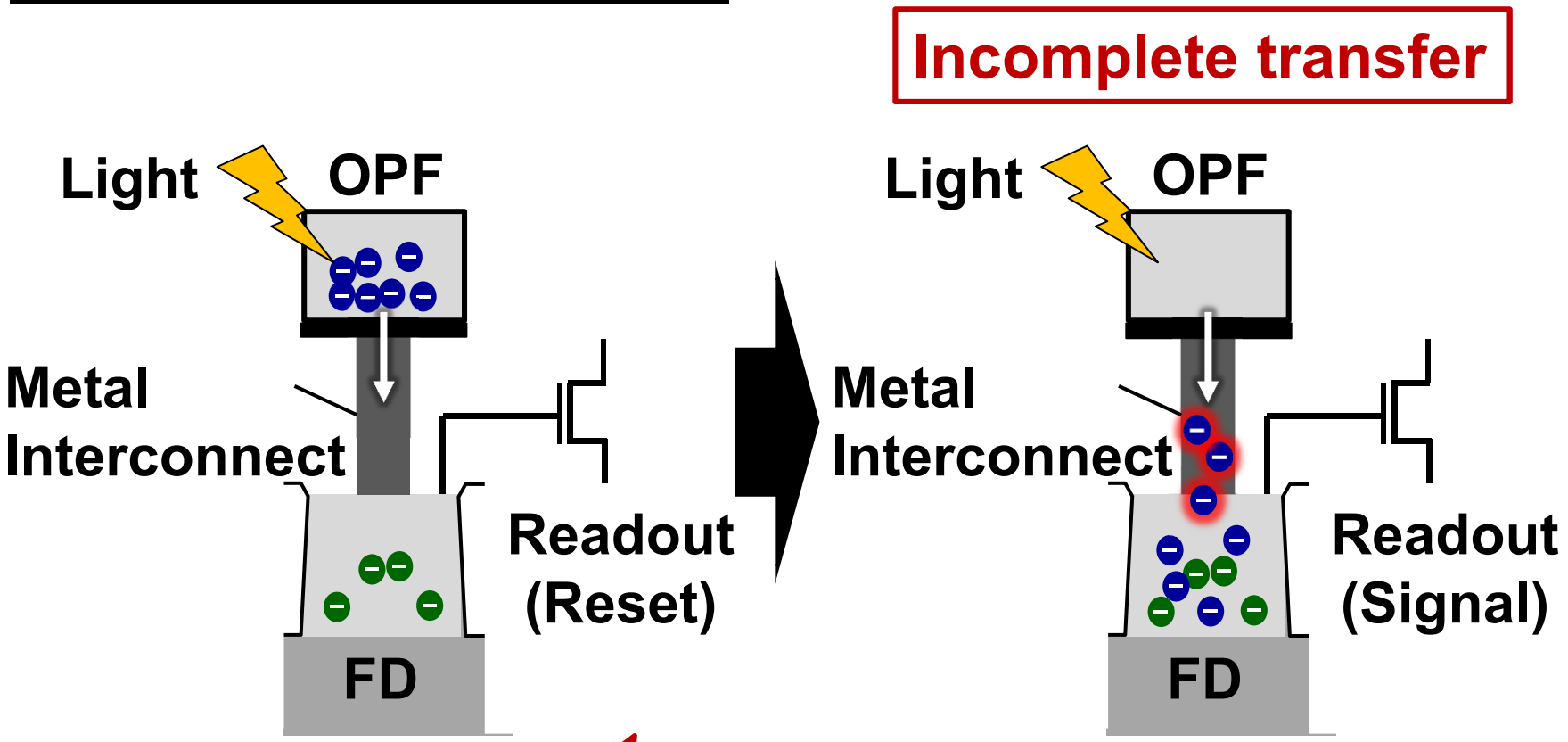
Reset Noise in Dark Region

OPF Image Sensor



Problem

Reset noise is left on the FD (include the Metal Interconnect)

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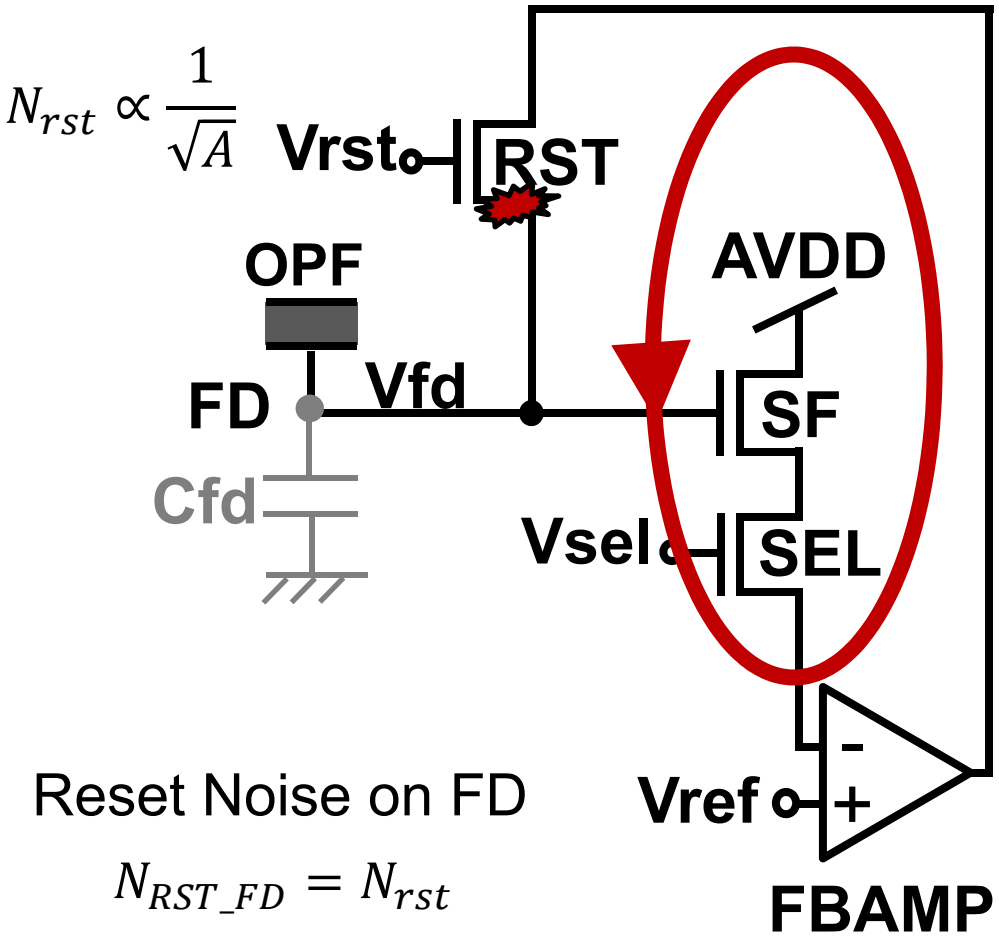
Conventional Noise Canceller

M.Ishii VLSI2013



Reset Noise on FD

$N_{RST\_FD} = N_{rst}$

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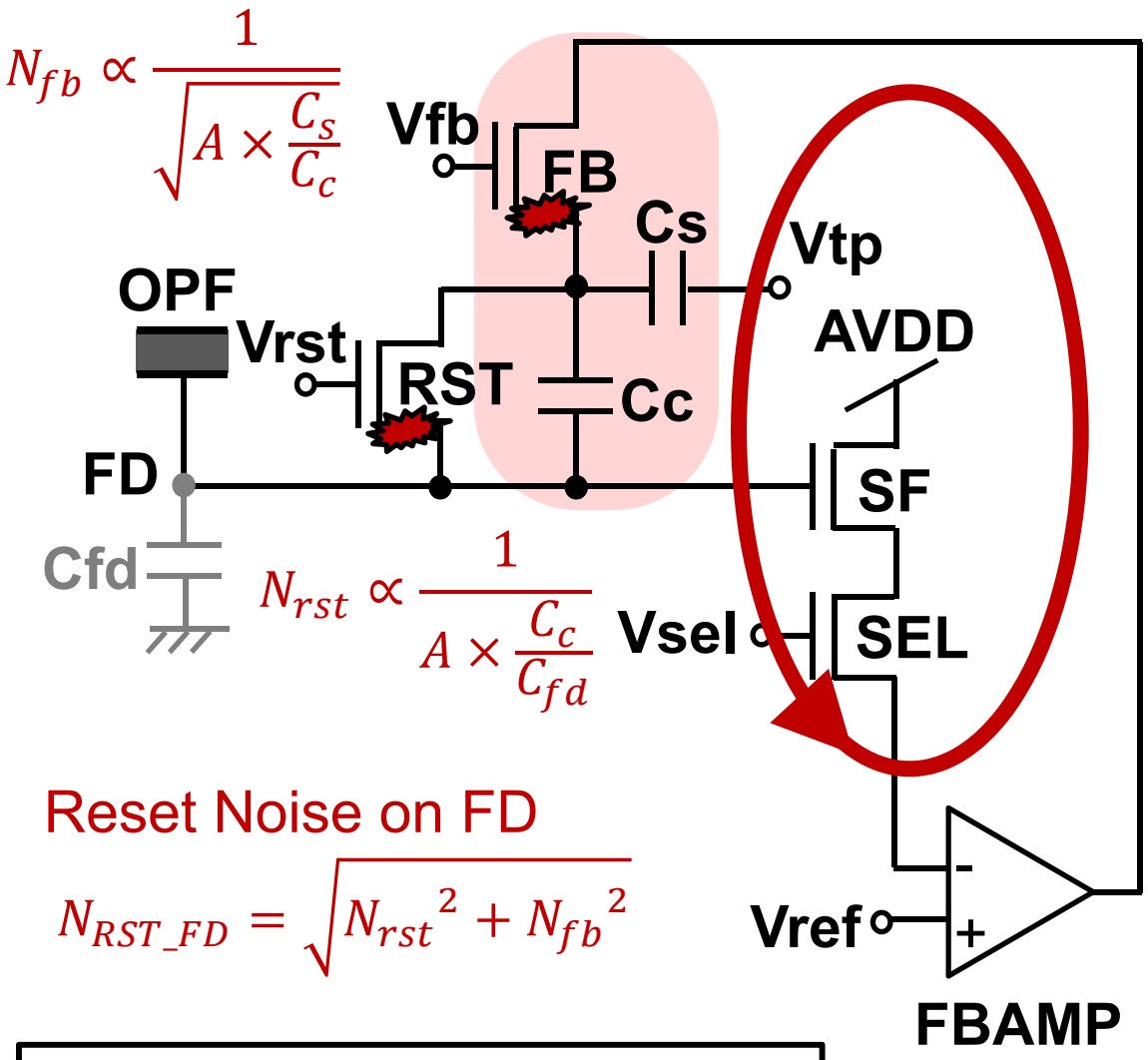
Capacitive-Coupled Noise Canceller



Negative Feedback Gain= -A

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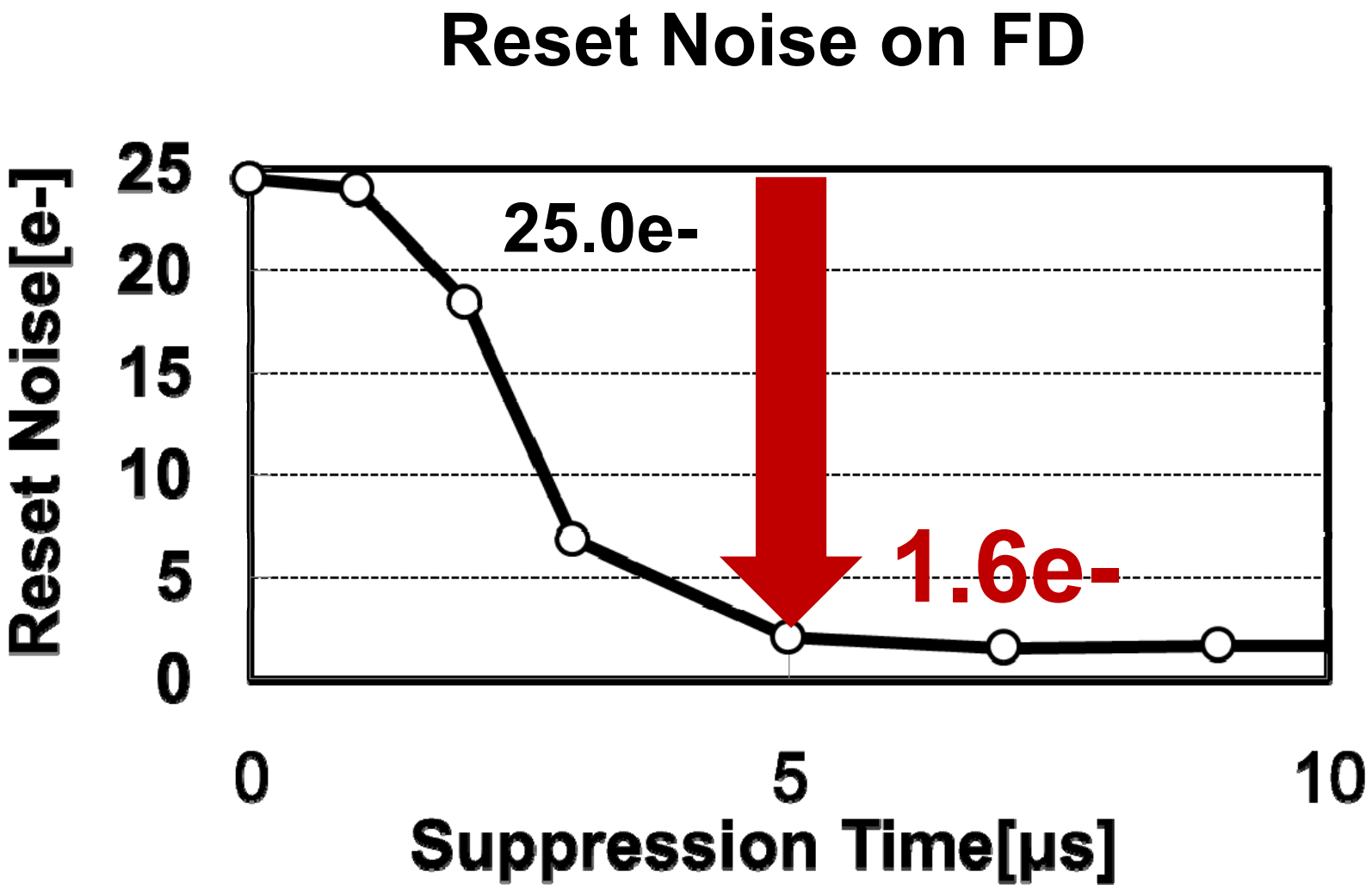
Result of Noise Cancellation



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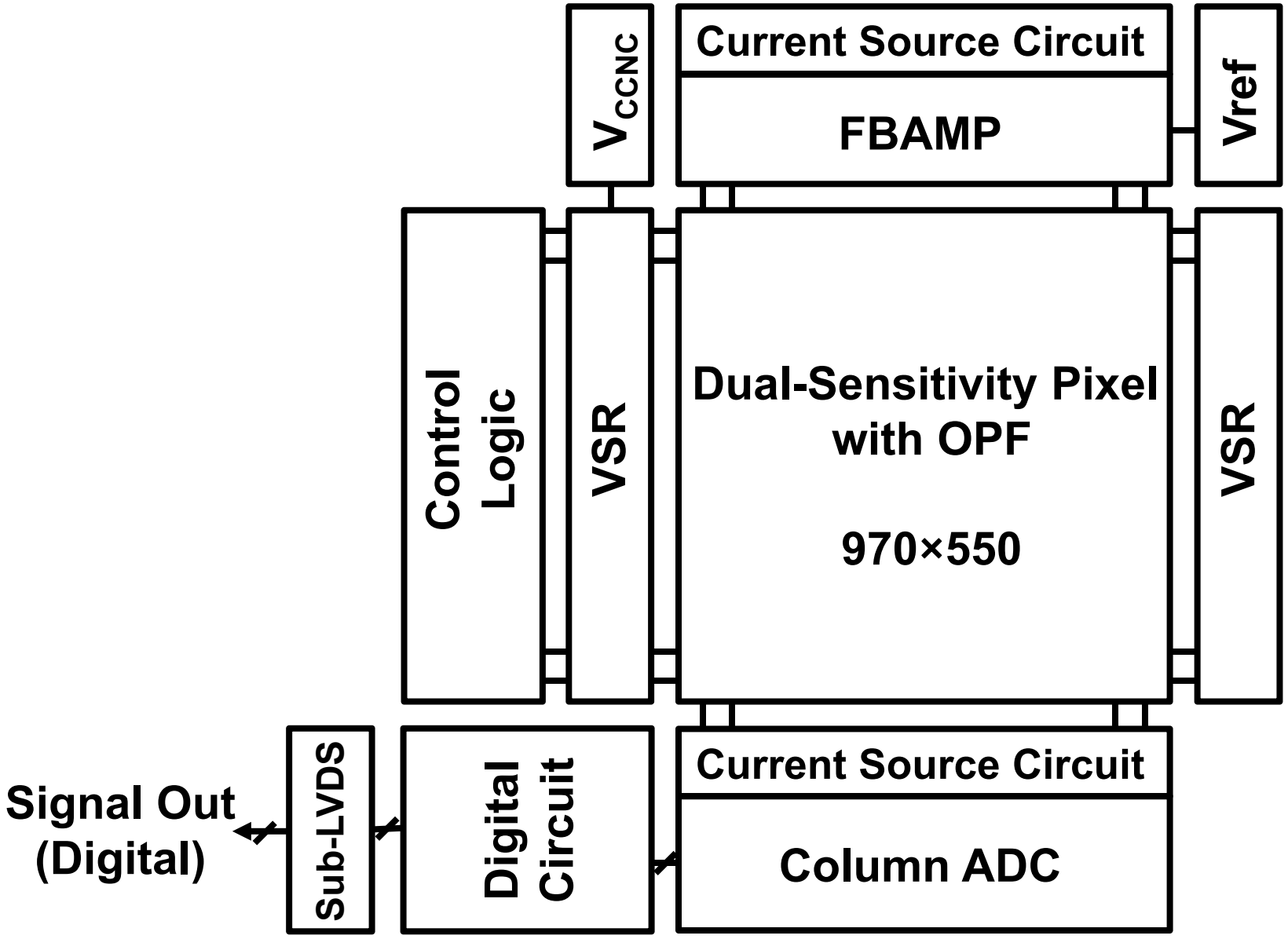
Block Diagram



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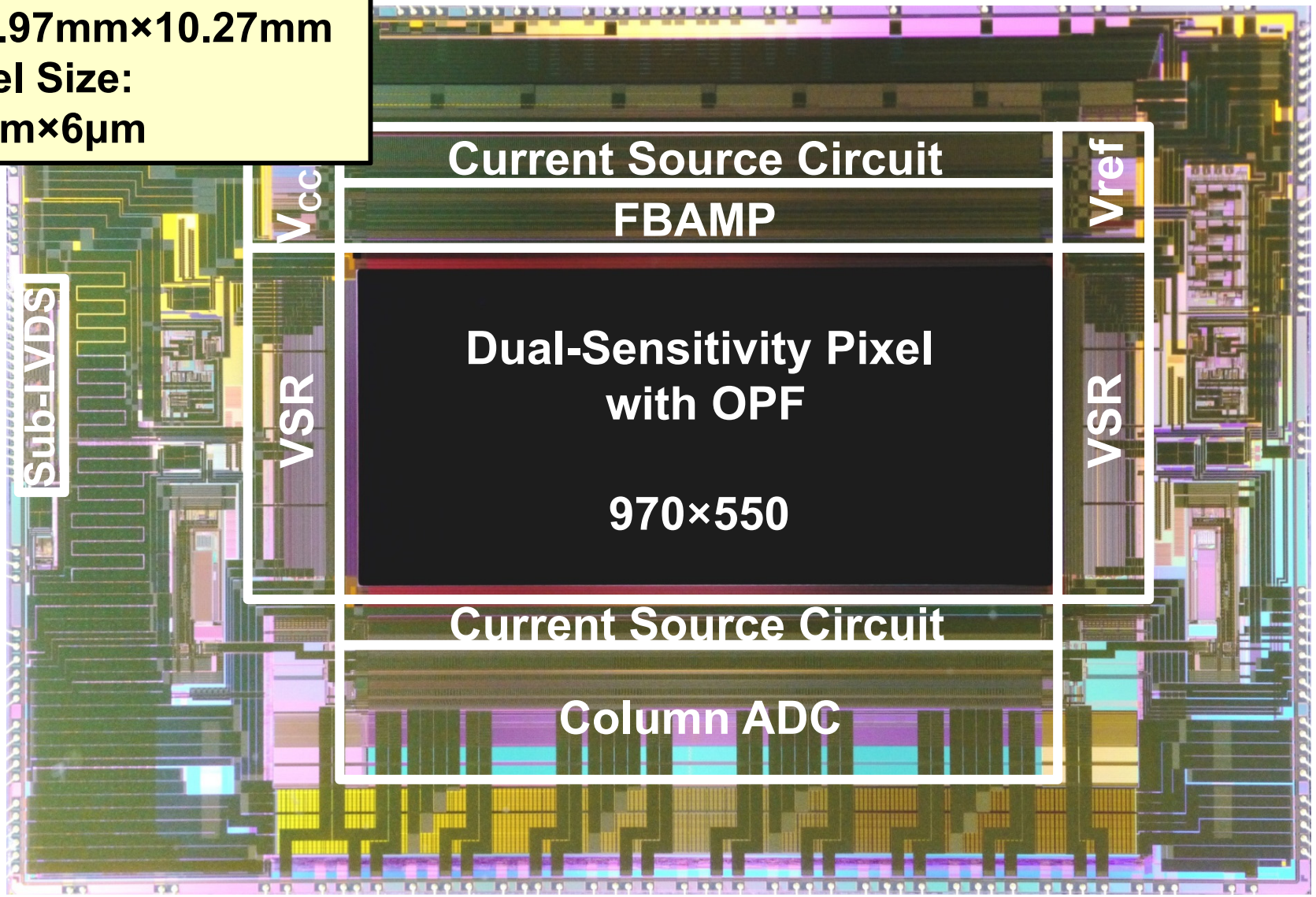
Chip Micrograph

Process:
65nm CMOS
Chip Size:
14.97mm×10.27mm
Pixel Size:
6μm×6μm



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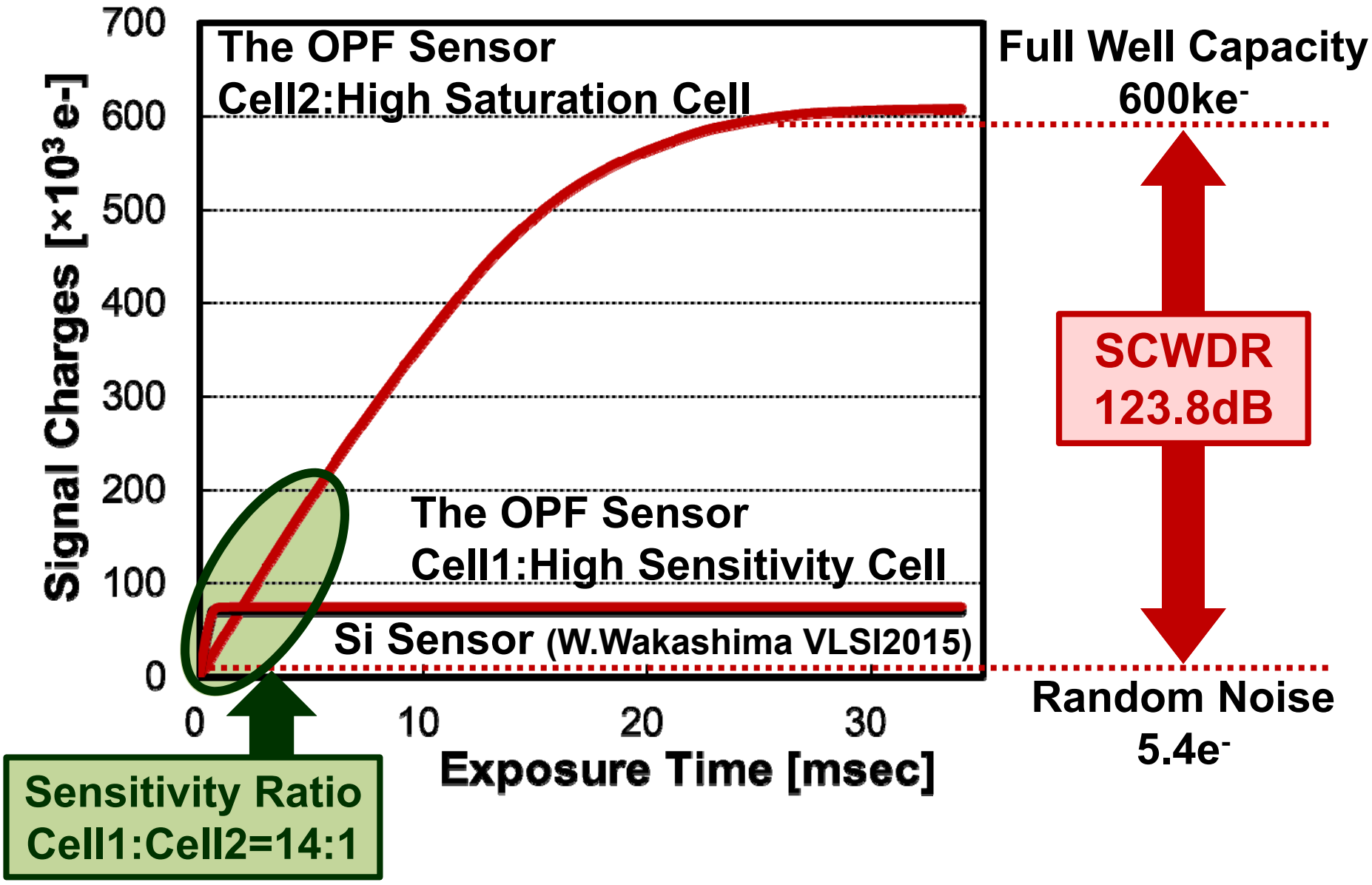
Photoelectric Conversion Characteristics



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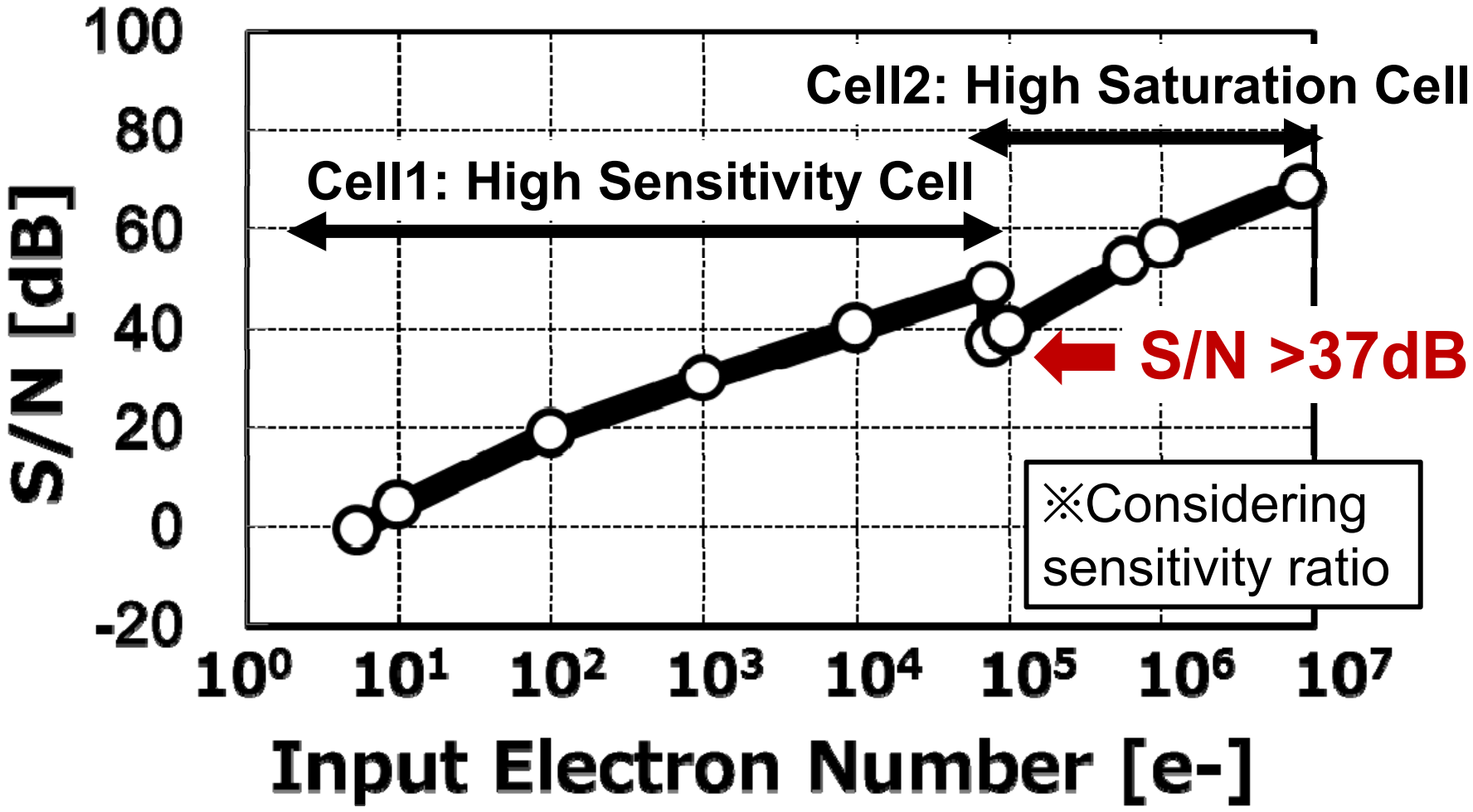
S/N Characteristics

- S/N at switching point is held >37dB.



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Simultaneous-Capture WDR Images

Simultaneous-Capture WDR

123.8dB

"High-Saturation Cell"

82.7dB

"High-Sensitivity Cell"

0dB

Image from the OPF image sensor

Weighting, using data from both cells

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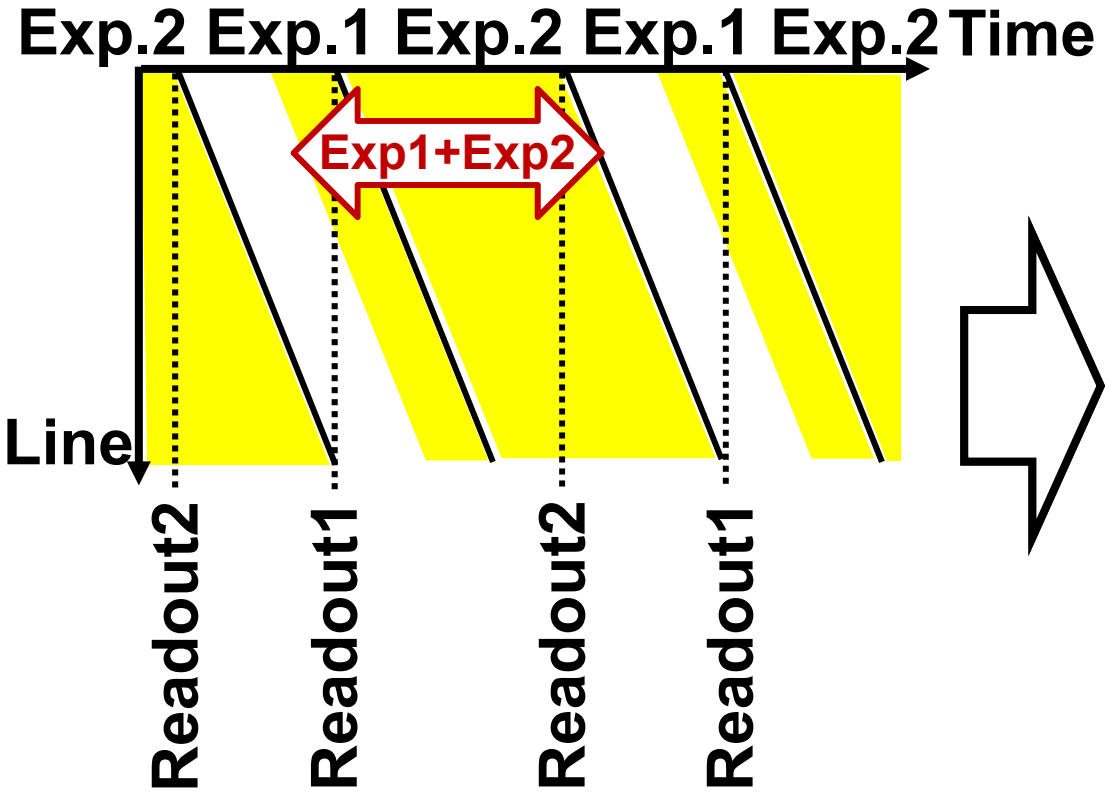
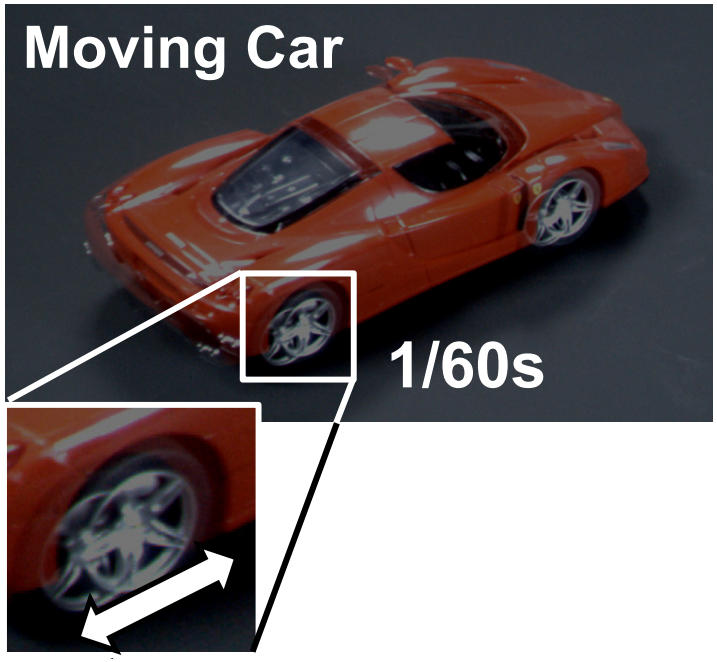
High-Speed Image (Conventional WDR)

➢ Motion blur of WDR is a big problem





Motion blur
at high-speed imaging

Synthesizing multiple exposures

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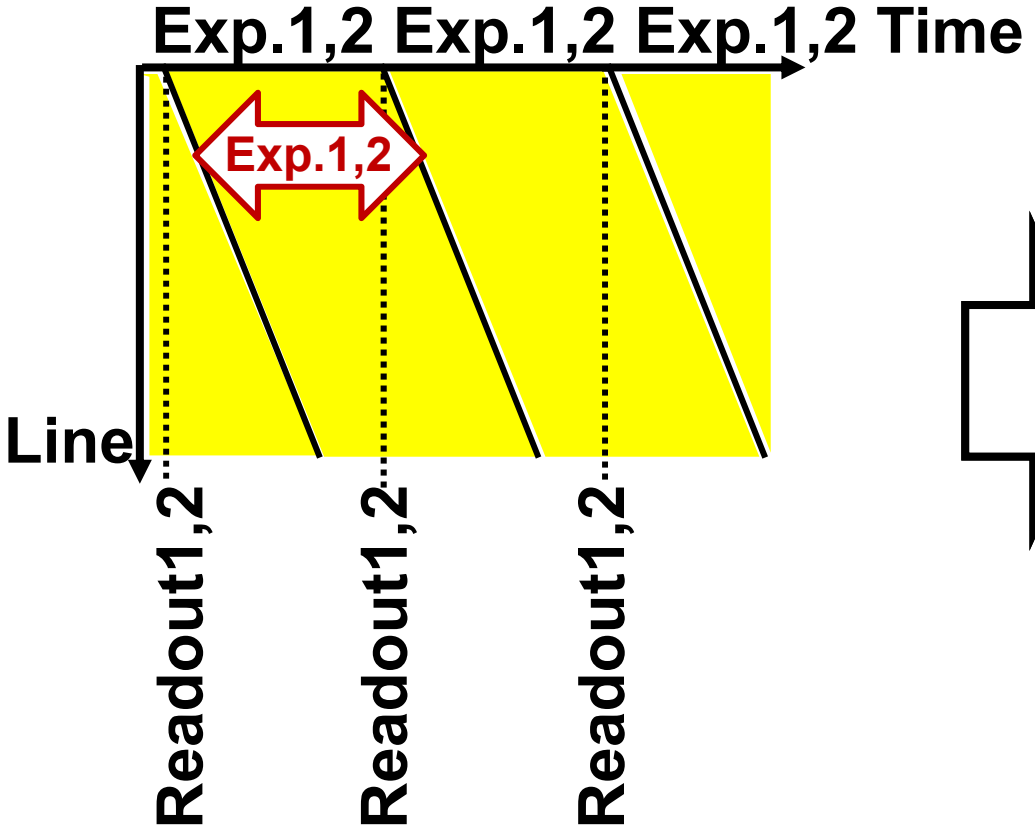
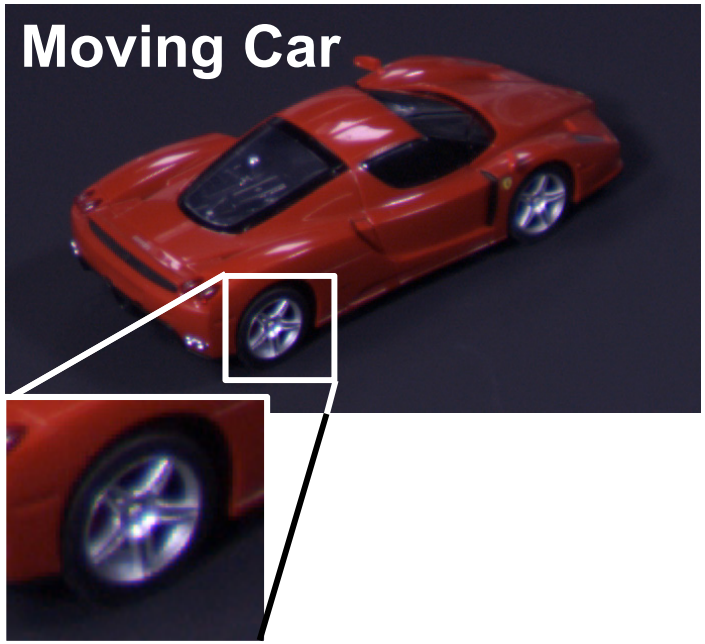
High-Speed Image (SCWDR)

- Motion blur is completely prevented
- Logic area can be small



Simultaneous exposures



No motion blur
at high-speed imaging

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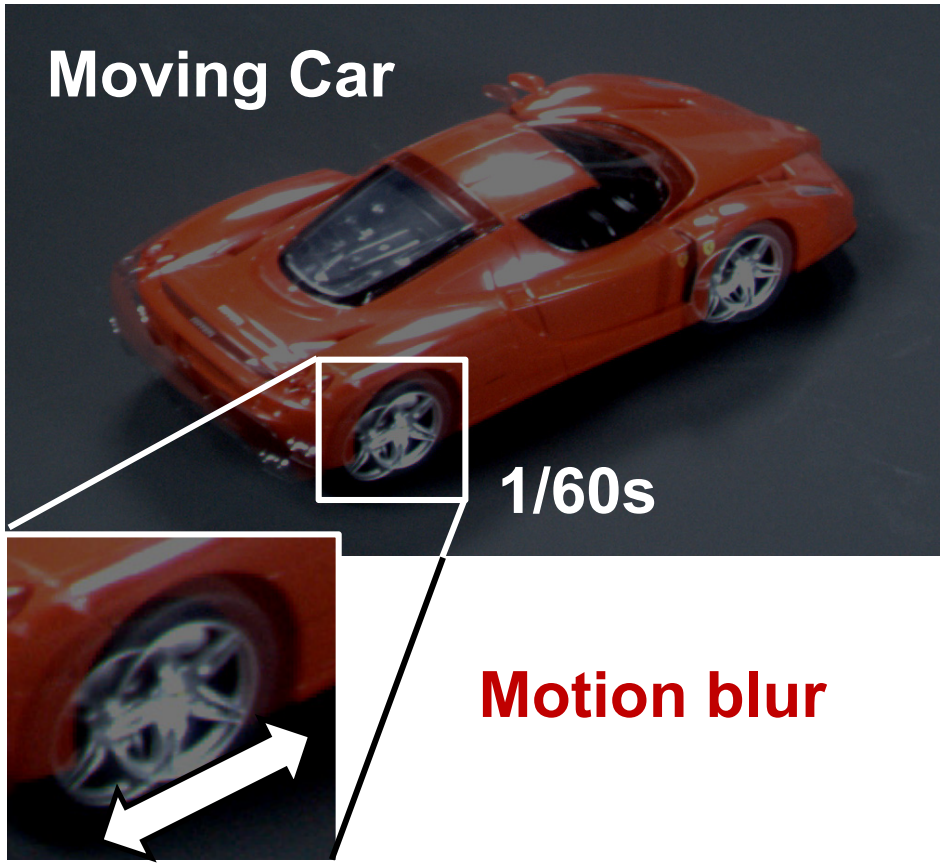
High-Speed Images

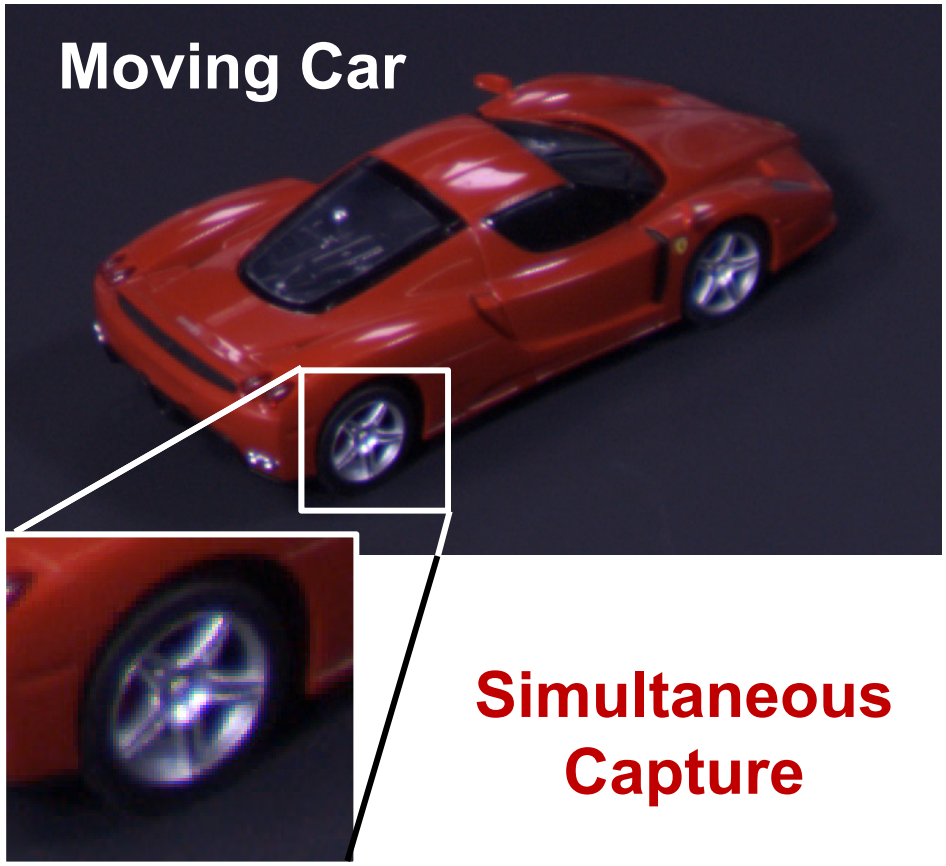
- **Motion blur is completely prevented**

Silicon Image Sensor



Motion blur

The OPF Image Sensor



Simultaneous Capture

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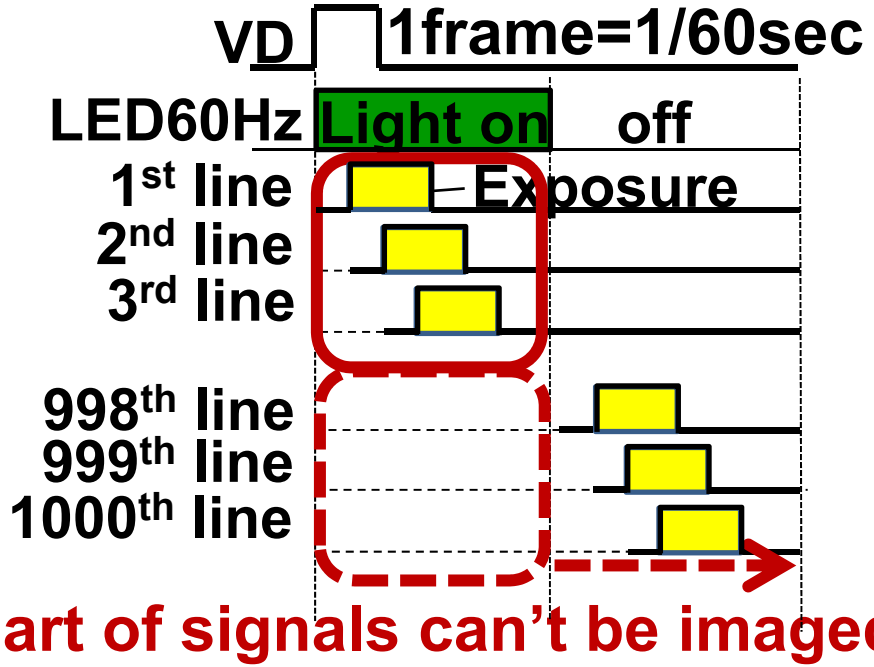
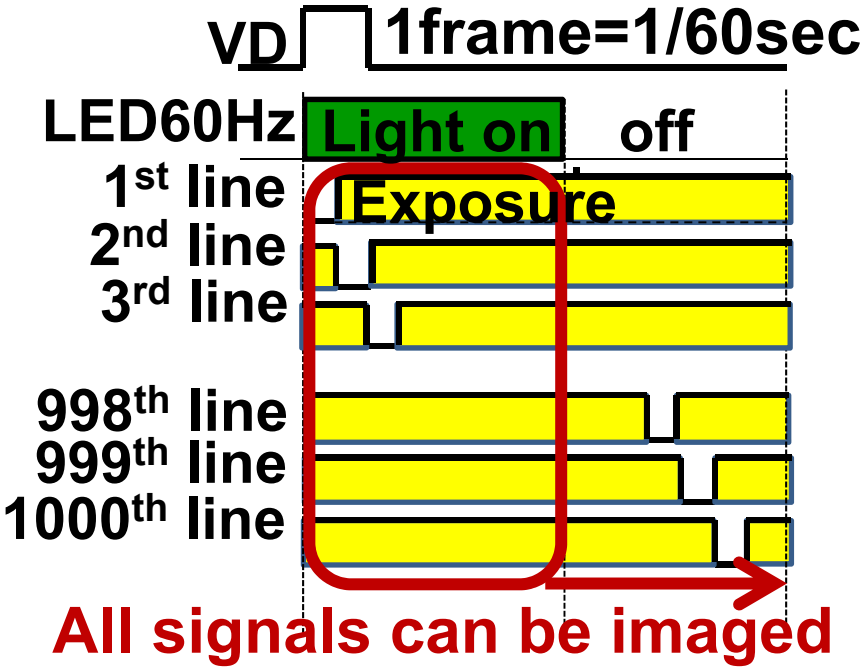
Prevention of LED Flicker

Silicon Image Sensor

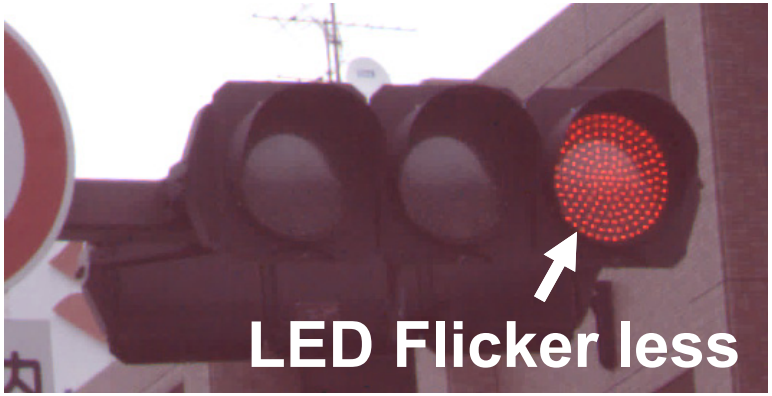


Part of signals can't be imaged

The OPF Image Sensor



All signals can be imaged



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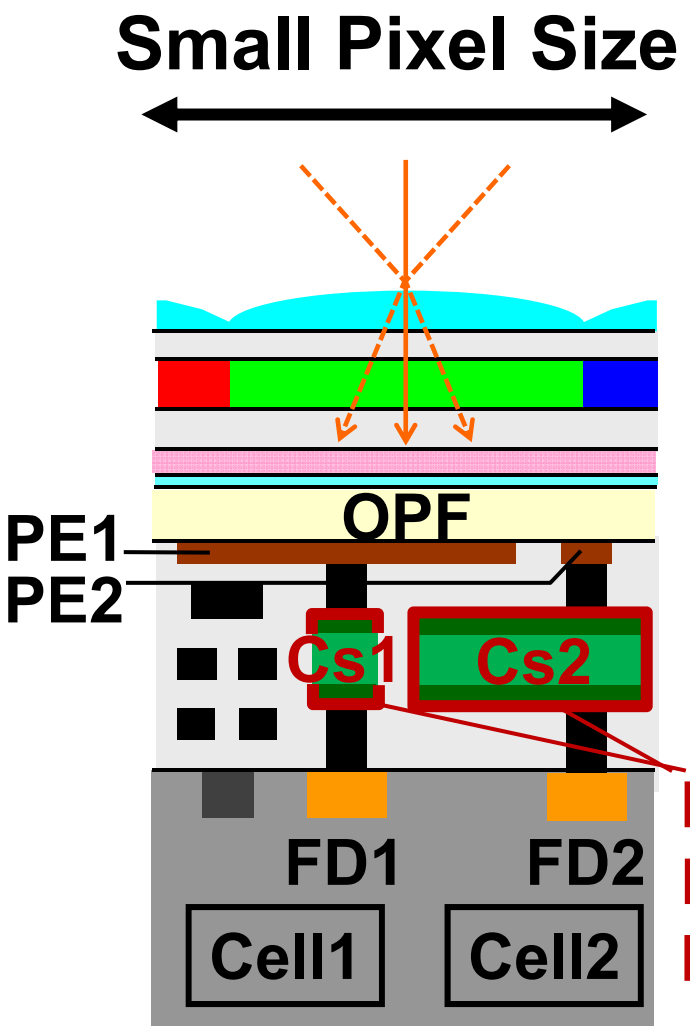
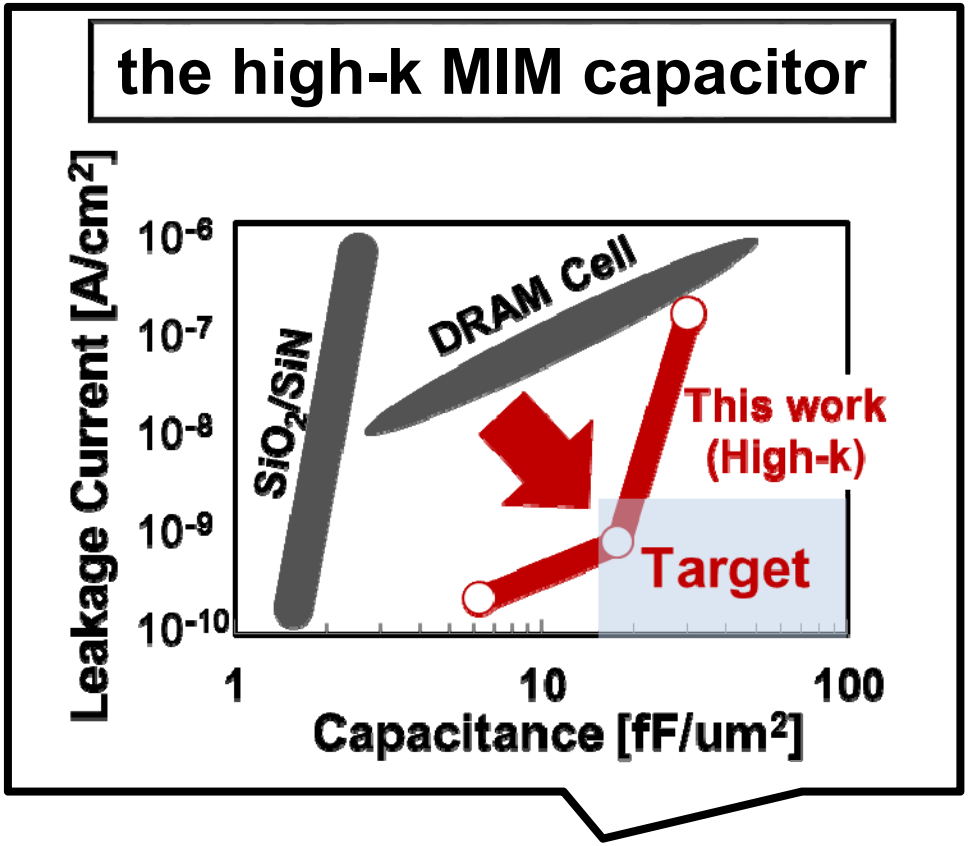
Layering of the High-k MIM Capacitor





High Capacitance:18fF/μm²
Low leakage Current:7.5×10⁻¹⁰A/cm²
MIM capacitor

High Sensitivity High Saturation

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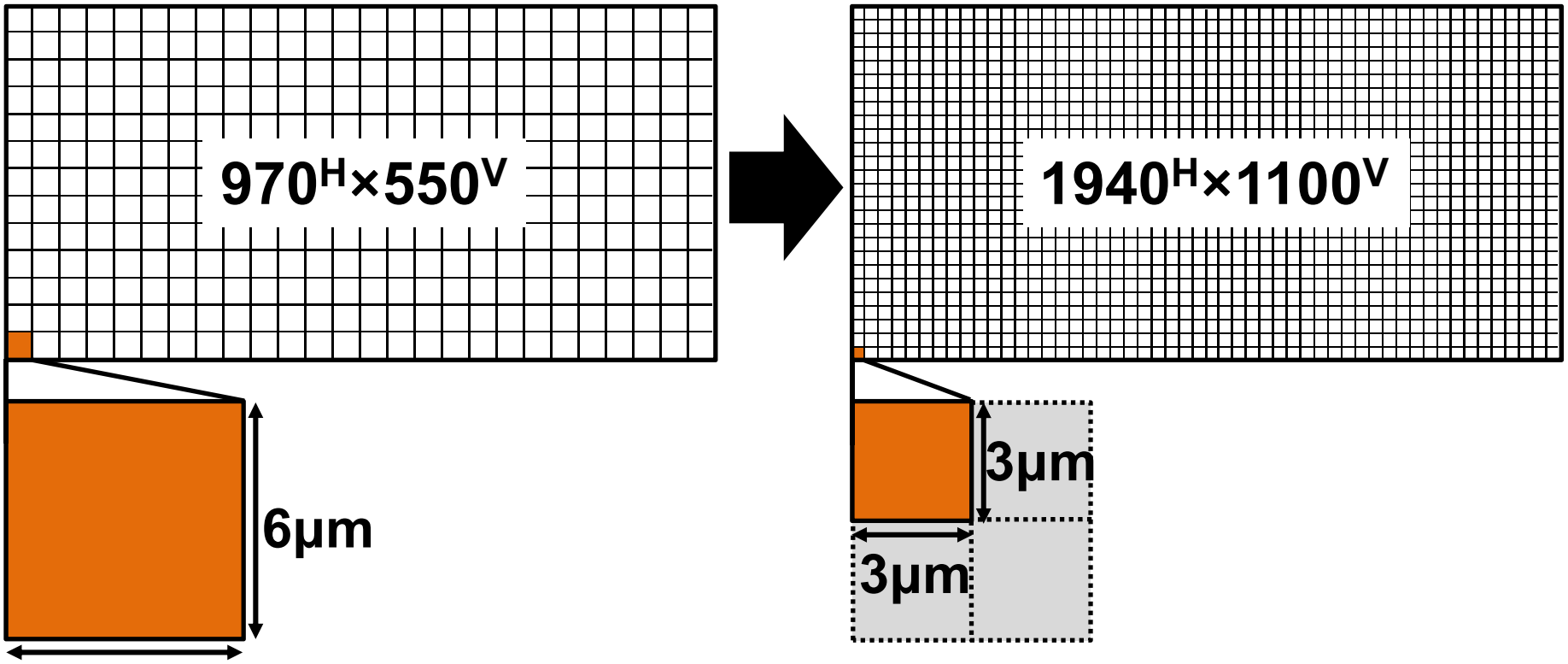
Pixel Size Shrink by the High-k MIM

Developing and Layering the High-k MIM Capacitor

Pixel Area



Pixel size can be reduced to×1/4

Resolution can be×4

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Outline

- Background
- Organic-Photoconductive-Film (OPF) CMOS Image Sensor
- Simultaneous-Capture Wide-Dynamic-Range
  - Dual-Sensitivity Pixel
- Reset Noise Cancellation
  - Capacitive-Coupled Noise Canceller
- Characterization Results
- Using MIM Capacitor
- **Conclusion**

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Performance Summary

*with MIM capacitor

	This work	A. Y. Chiou VLSI 2015	W. Wakashima VLSI 2015	N. Akahane ISSCC 2006
Chip Size [mm^2]	14.9×10.2	---	5.4×1.8	2.6×2.6
Pixel Size [μm^2]	**6×6** *3×3	7.6×7.6	5.5×5.5	20×20
Number of Pixels	**970×550** *1940×1100	96×96	360×1680	64×64
Frame Rate [fps]	**60**	15	---	---
CMOS Process	65nm	0.18μm	0.18μm	0.35μm
SCWDR [dB]	**123.8**	87	104	100
Full Well Capacity [e$^-$]	**600k**	---	76k	---
Random Noise [e$^-$]	5.4	---	0.46	---
Reset Noise [e$^-$]	**1.6**	---	---	---

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Conclusion

We have Developed the OPF CMOS image sensor with the new pixel structures

- Dual-Sensitivity Pixel
- Capacitive-Coupled Noise Canceller

Simultaneous-Capture WDR:123.8dB is achieved

This OPF image sensor will contribute to the high-speed imaging & sensing applications!

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Acknowledgement

We would like to thank FUJIFILM Corporation for providing organic semiconducting materials.

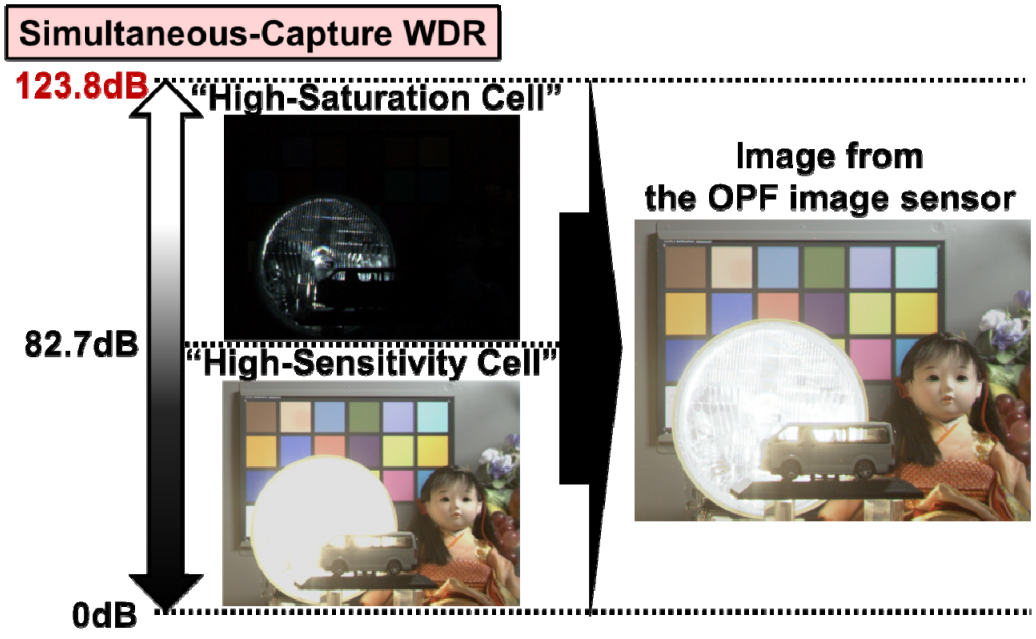
We would like to thank engineers in Panasonic Semiconductor Solution Co. for supporting chip design.

And, we would like to express special thanks to Yoshiyuki Matsunaga for encouragement and discussion throughout this work.

Thank you for your attention !

ISSCC 2016 Demonstration Sessions

February 1, 2016: 5:00 – 7:00 pm Golden Gate Hall



DS1

Panasonic

210ke- Saturation Signal 3μm-pixel Variable Sensitivity Global Shutter Organic Photoconductive Image Sensor for Motion Capture

Sanshiro Shishido, Yasuo Miyake, Yoshiaki Sato, Tokuhiko Tamaki, Naoki Shimasaki, Yoshihiro Sato, Masashi Murakami, Yasunori Inoue

Advanced Research Division,
Panasonic Corporation

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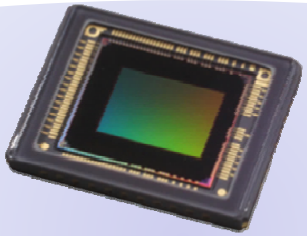
Background



Medical

In-vehicle

"Key Device"

Mobile

Surveillance

Broadcast

DSL

Robot vision

Needs for "Imaging" & "Sensing"

- WDR
- High Sensitivity
- High Speed
- High Functional

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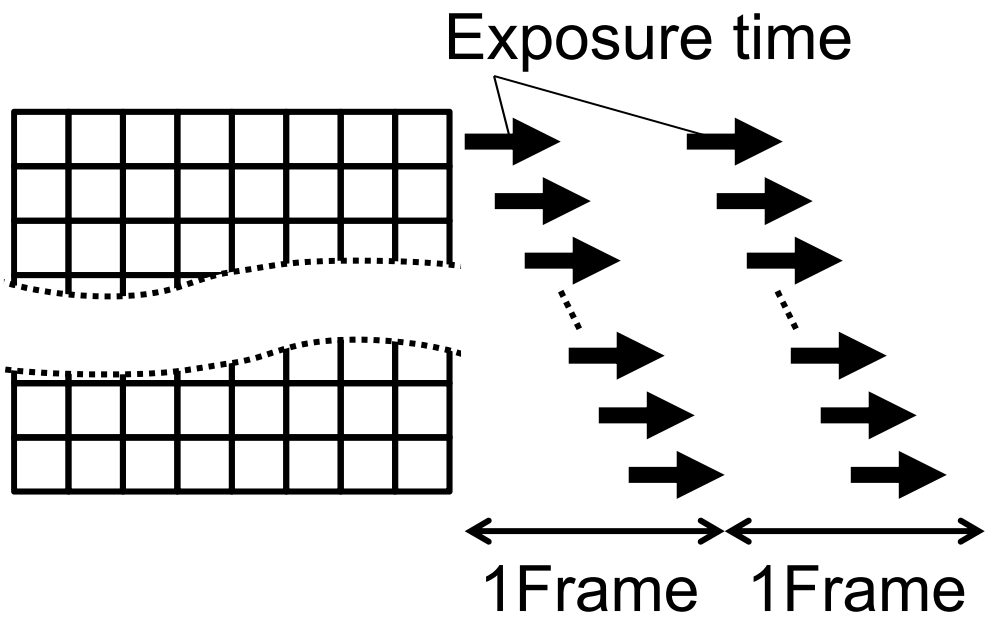
Rolling Shutter & Global Shutter

Shutter distortion

Flash banding

Rolling Shutter Operation



⇒Global Shutter (GS) solves such deformation

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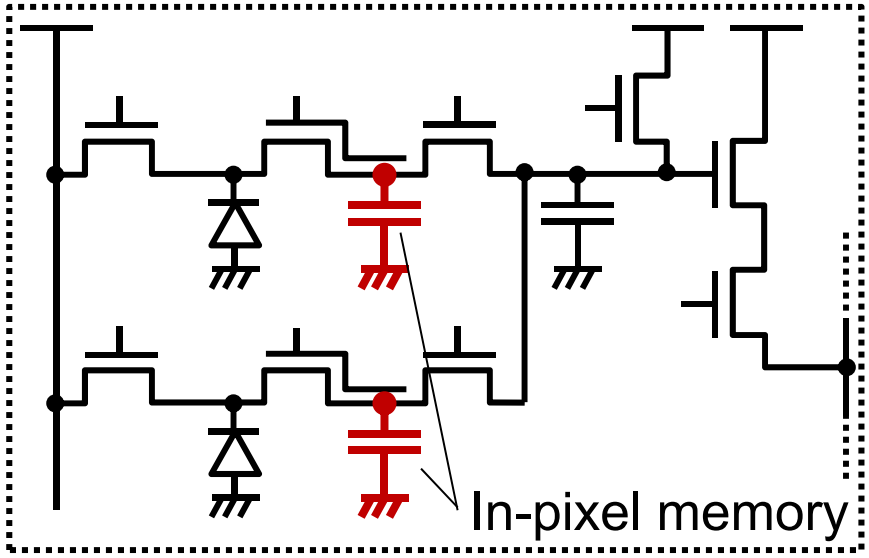
Issues on GS Pixel

CIS GS pixel

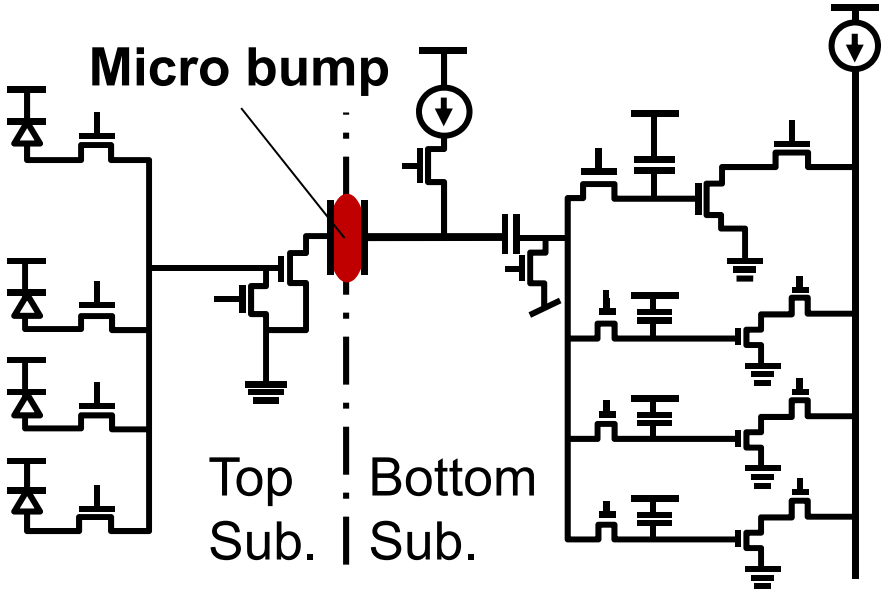
[1]M.Sakakibara, ISSCC2012



In-pixel memory limits saturation signal

3D Stacked CIS GS pixel

[2]T.Kondo, VLSI2015



Bump pitch limits pixel size (shared pixel is needed)

Conventional GS has issues on Pixel size/Saturation signal

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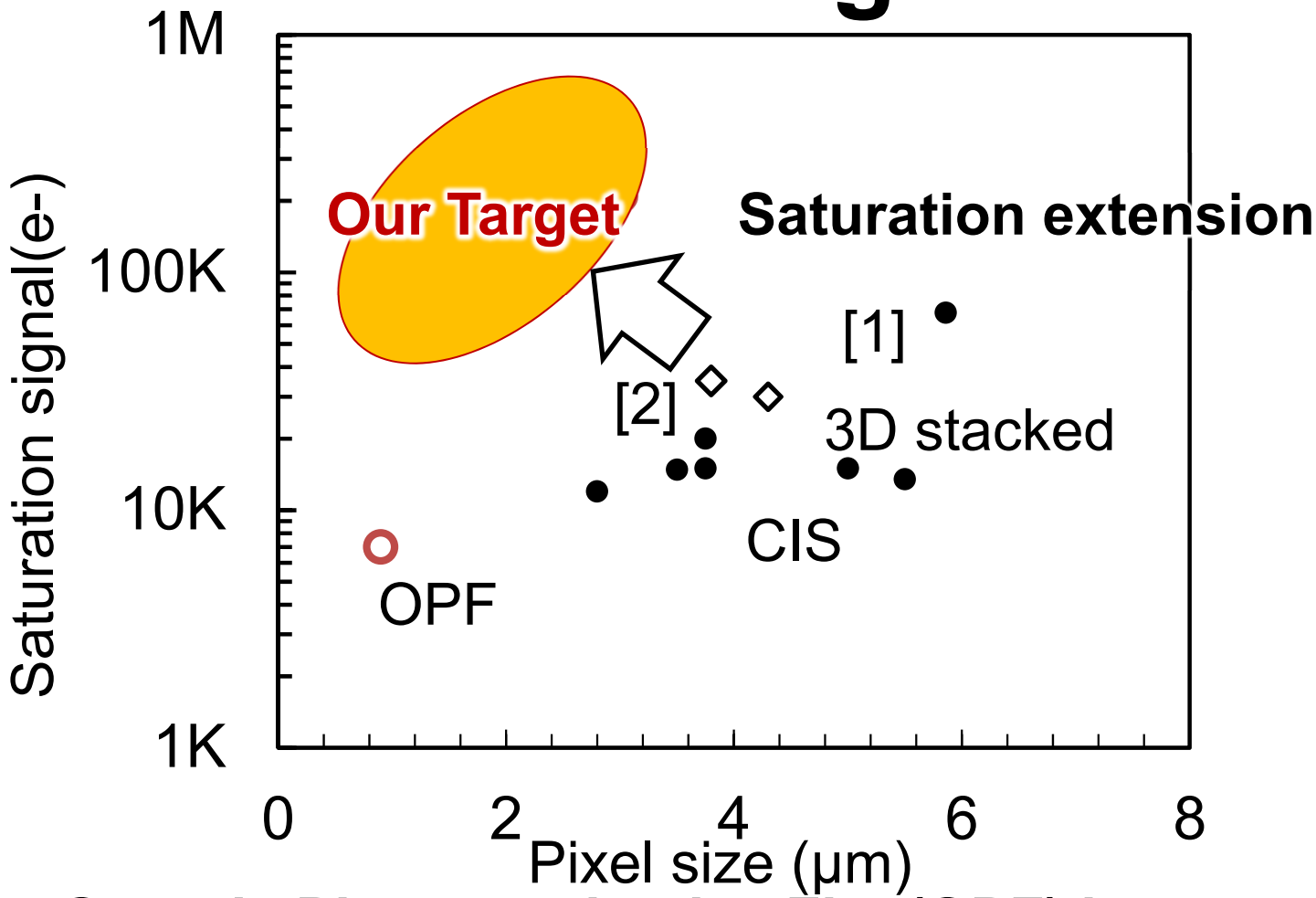
Our Target



By Organic Photoconductive Film(OPF) image sensor

- To extend GS performance (saturation extension)
- To develop new sensing functions

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Key Technologies

1. Global Sensitivity Control by OPF Sensor
2. High Saturation GS pixel
3. High Speed Reference Readout for OPF Sensor
4. Variable Sensitivity GS

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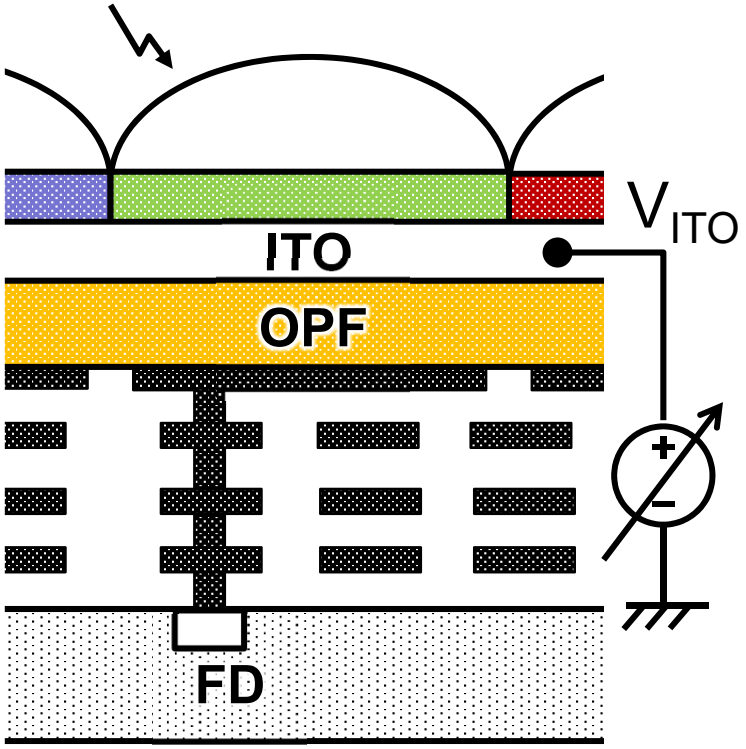
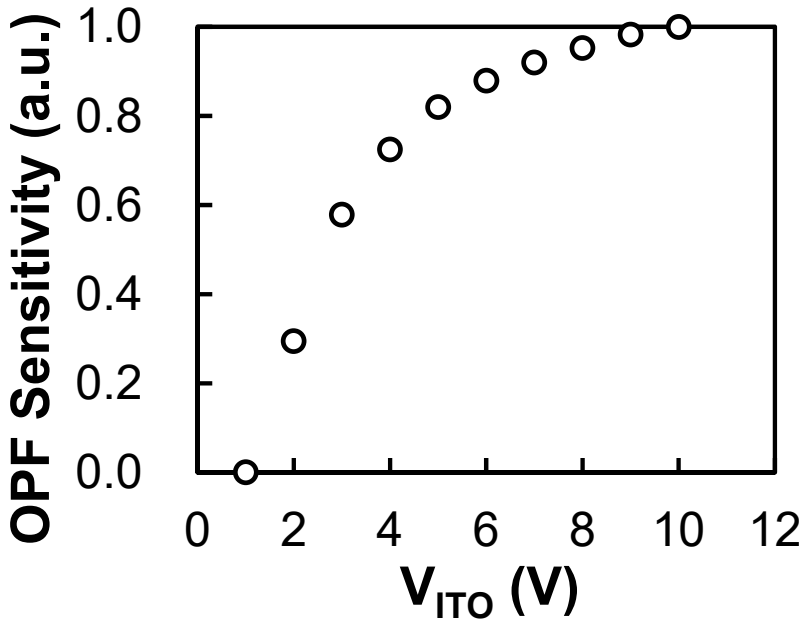
GS of OPF Image Sensor

Photoelectric conversion controlled (PCC) GS

(M.Takase, IEDM2015)





- Good for saturation extension (No in-pixel memory)
- Global sensitivity can be controlled

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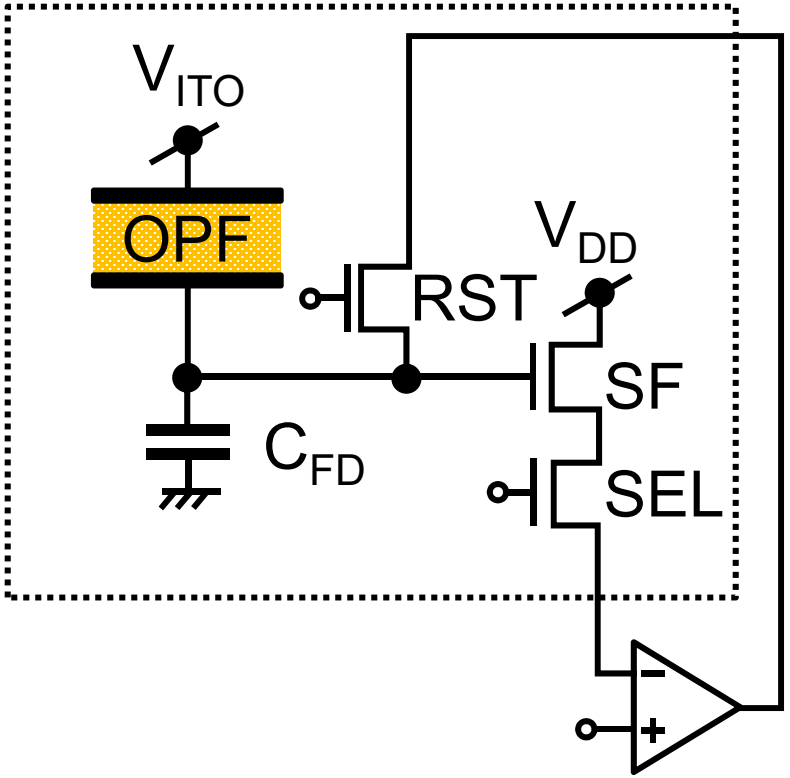
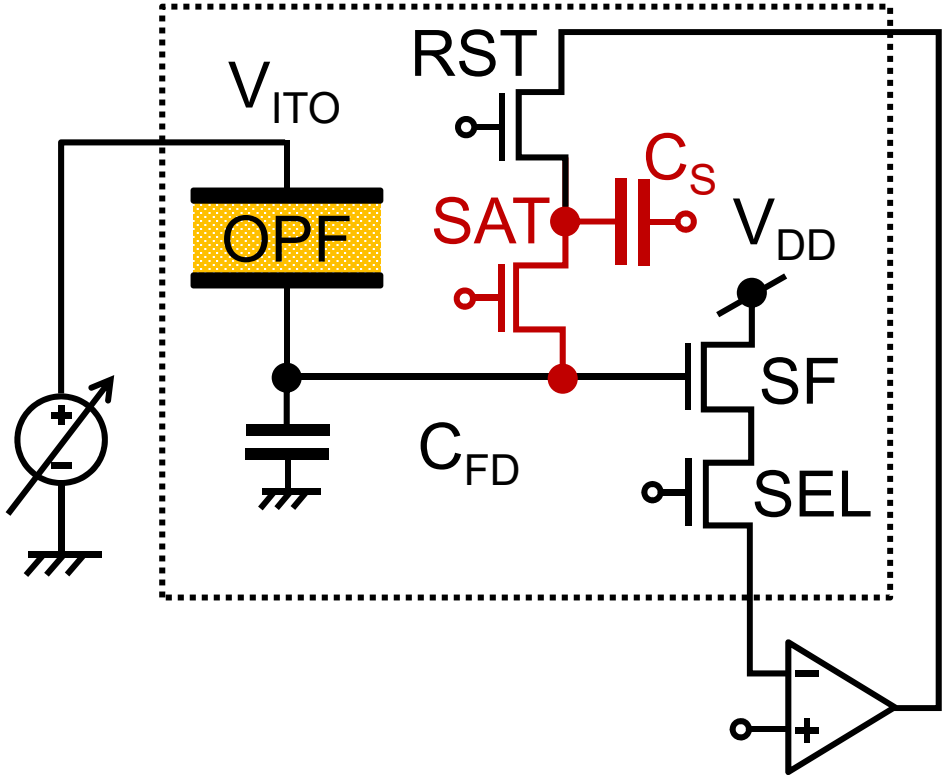
High Saturation GS pixel

Previous work



This work



A key feature of OPF sensor:
allows additional pixel circuits

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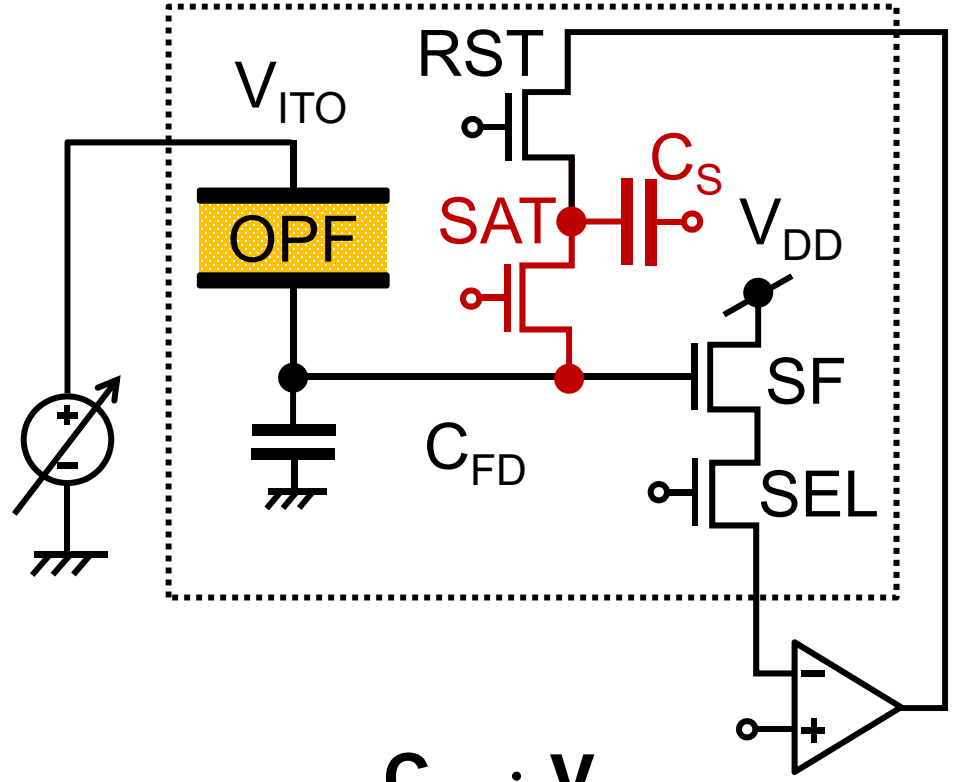
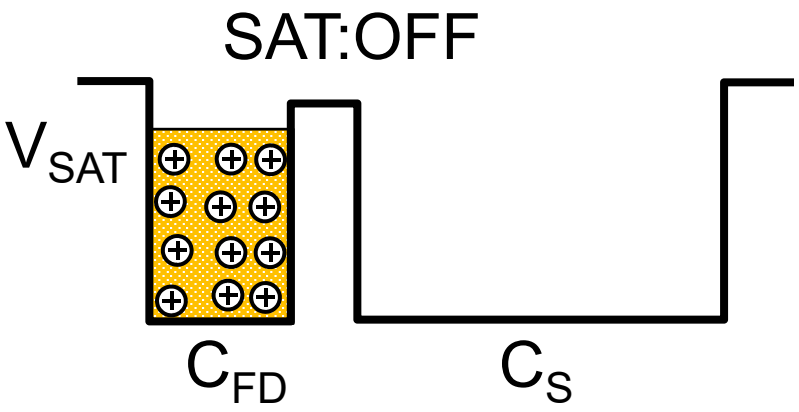
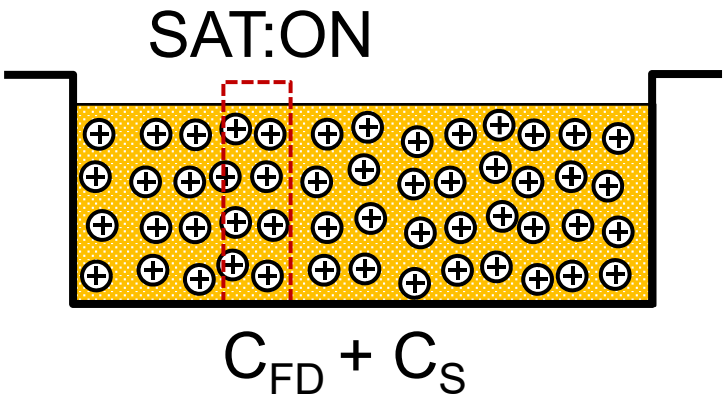
High Saturation GS pixel



High gain for SNR



High saturation



$$Q_{SAT\_OFF} = \frac{C_{FD} \cdot V_{SAT}}{q}$$

$$Q_{SAT\_ON} = \frac{(C_{FD} + C_S) \cdot V_{SAT}}{q}$$

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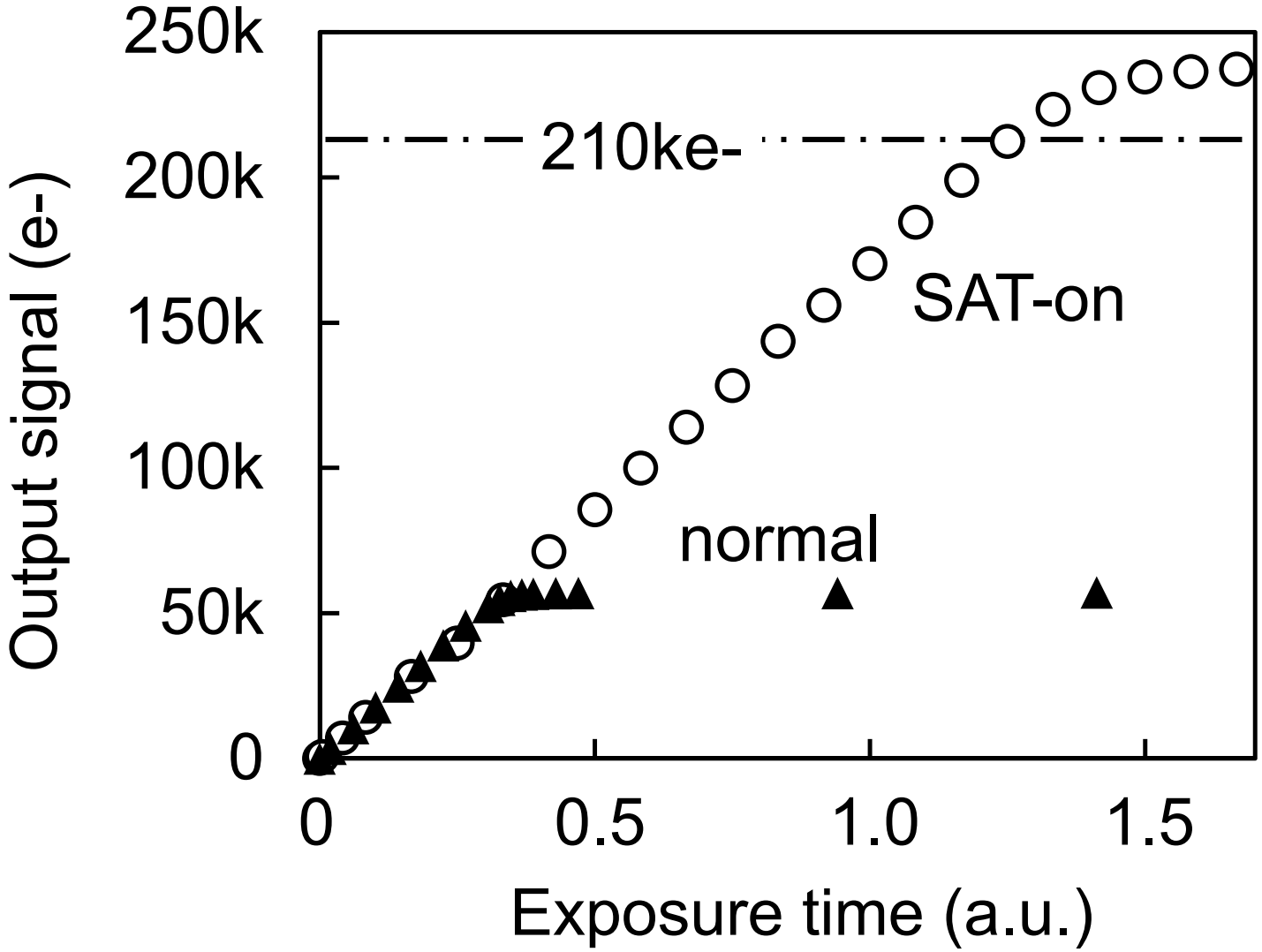
Response Curve



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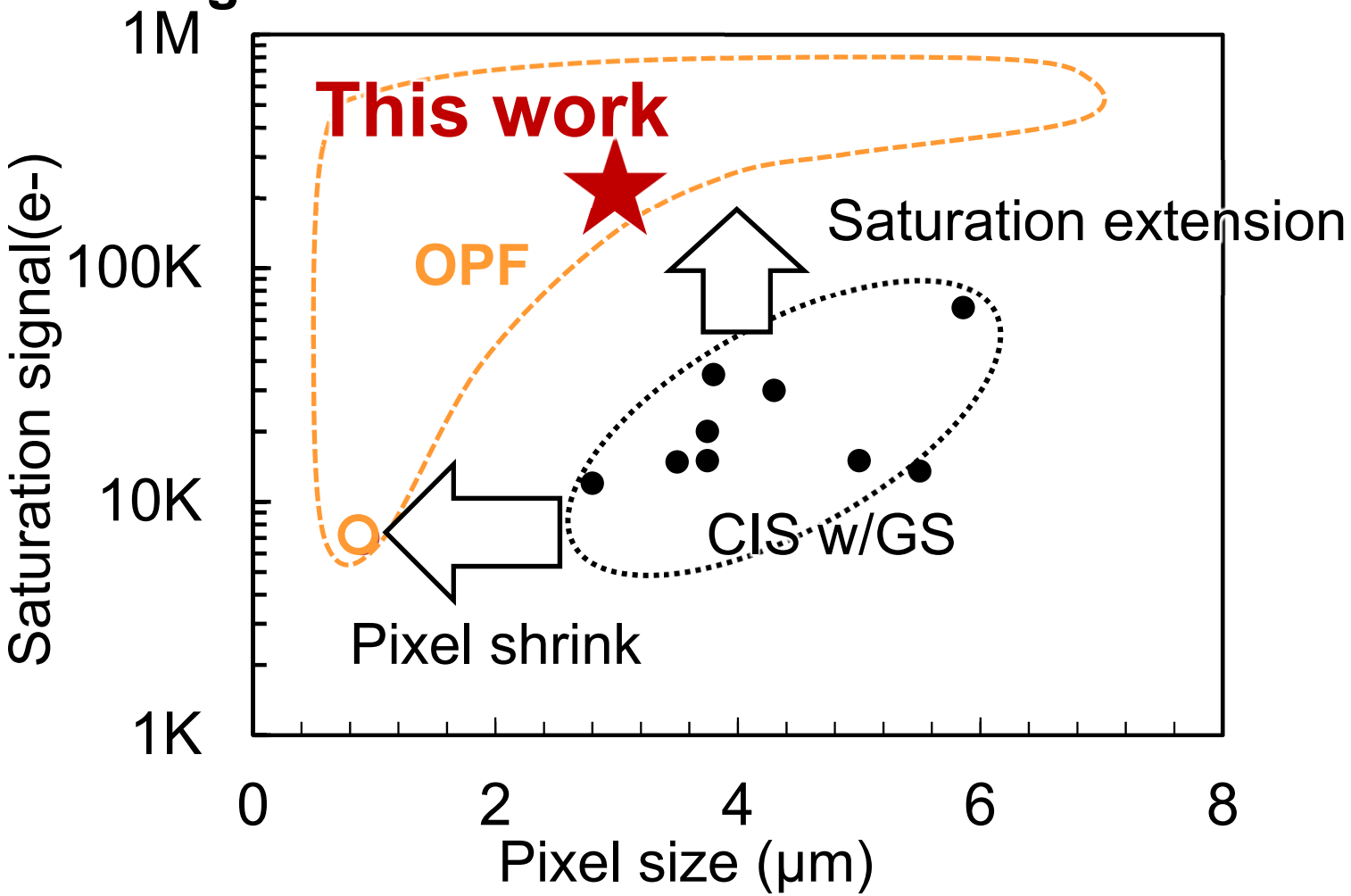
Benchmarking

Image sensors with Global Shutter function



High saturation GS pixel by OPF sensor is achieved

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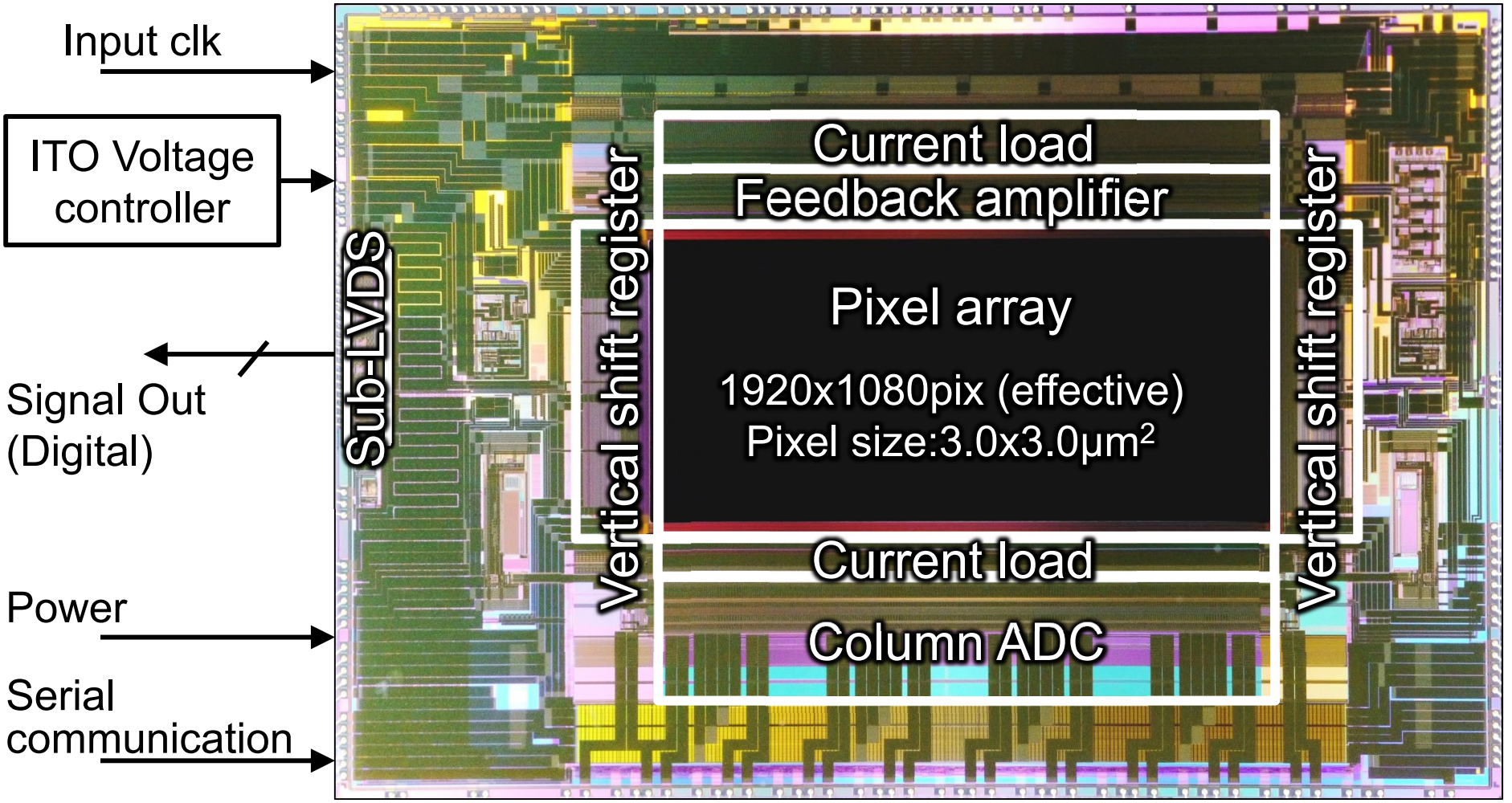
Chip Micrograph



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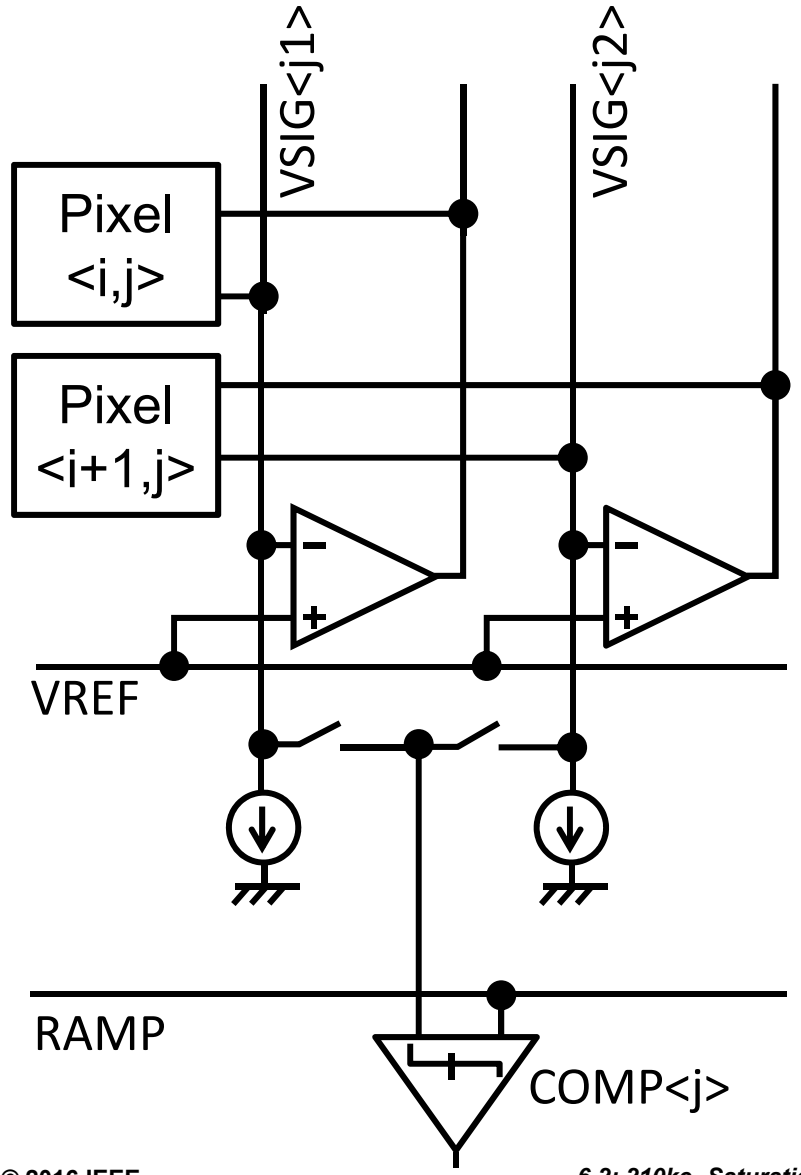
High Speed Reference Readout



- Column FB reset is executed
- 2 VSIG/column is used for
  - readout (signal & reset level)
  - e-shutter

Column line access limits Readout speed

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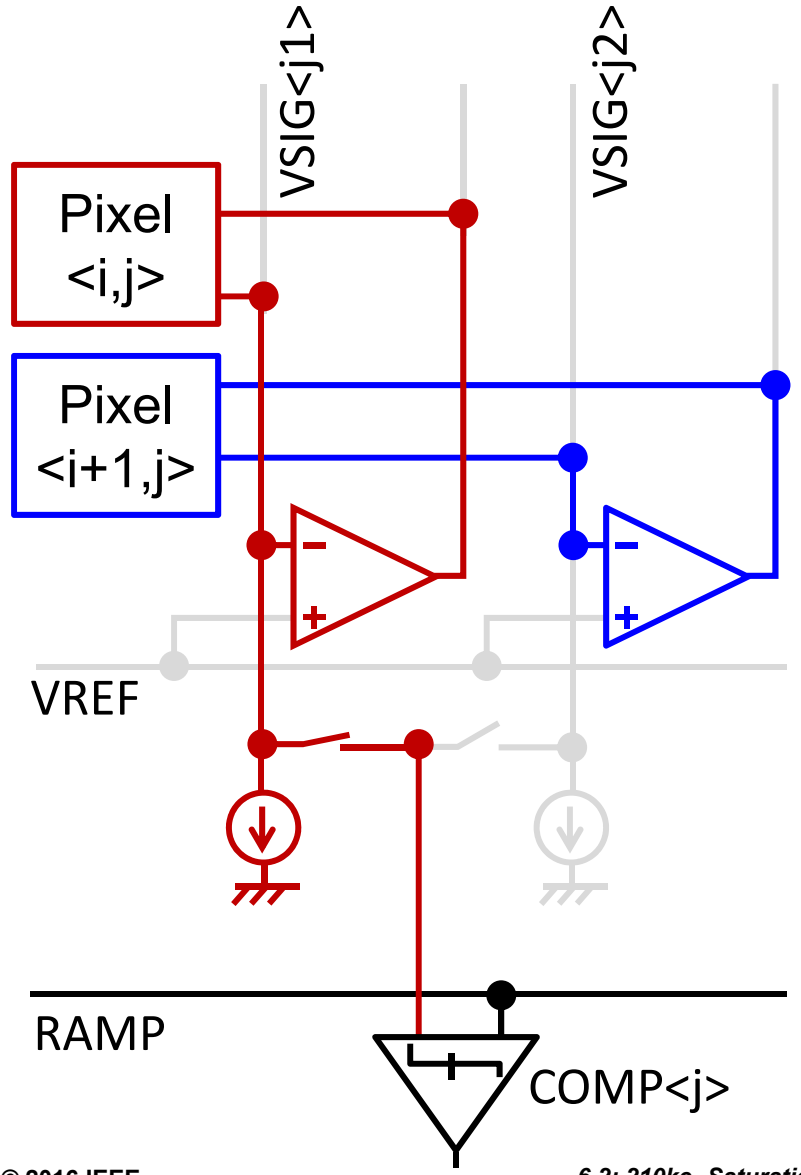
High Speed Reference Readout



- Column FB reset is executed
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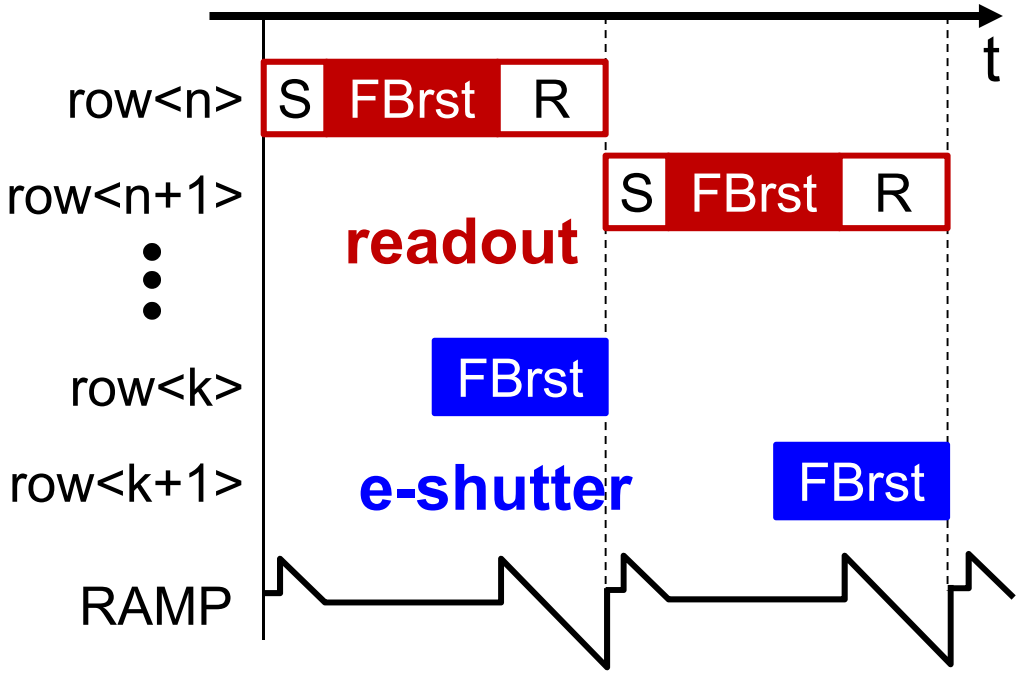
  - readout (signal & reset level)
  - e-shutter



Column line access limits Readout speed

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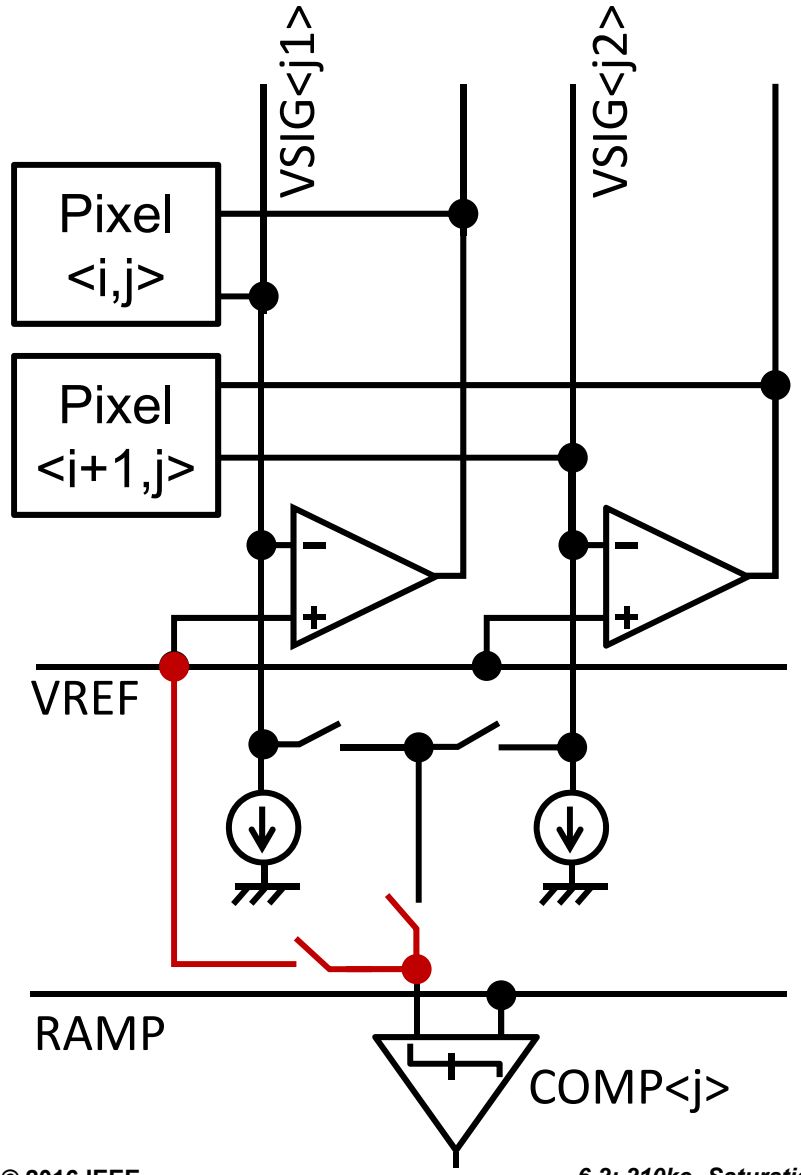
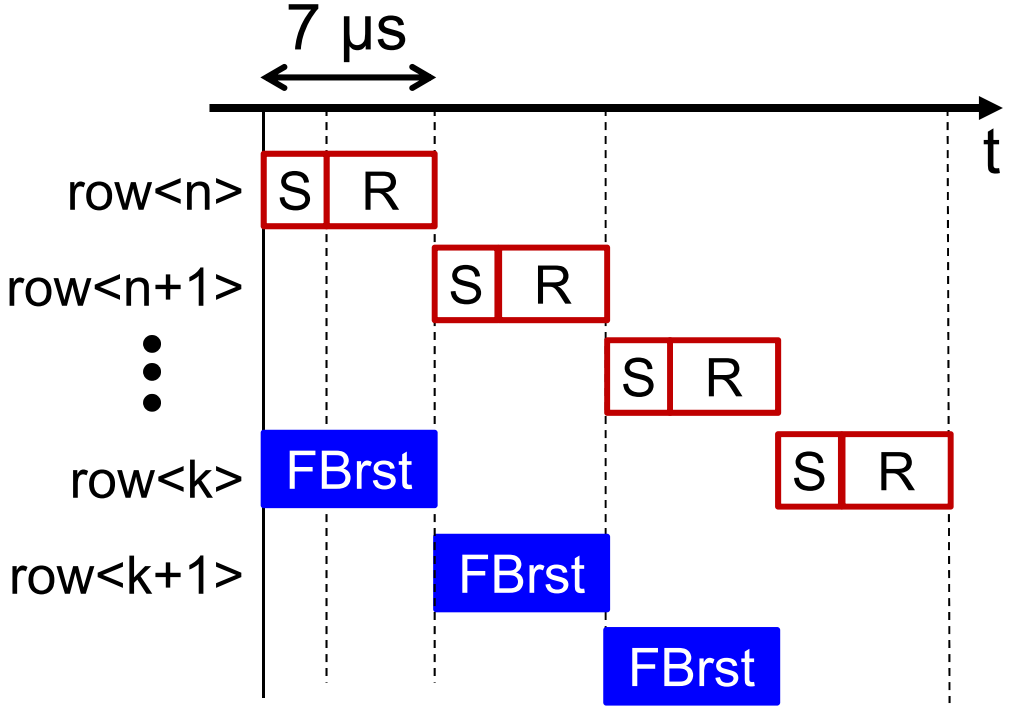
High Speed Reference Readout



Pixel-separated reference readout is executed for high speed read



H cycle can be shortened from 14 µs to 7 µs

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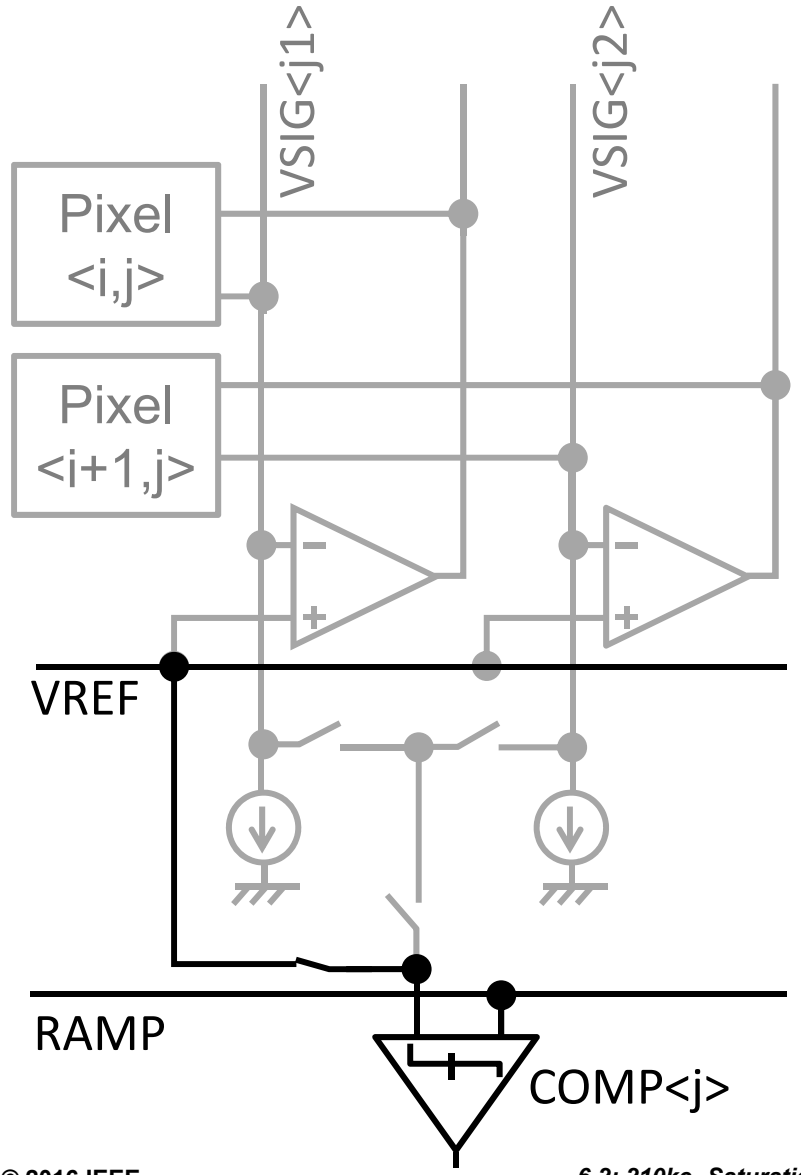
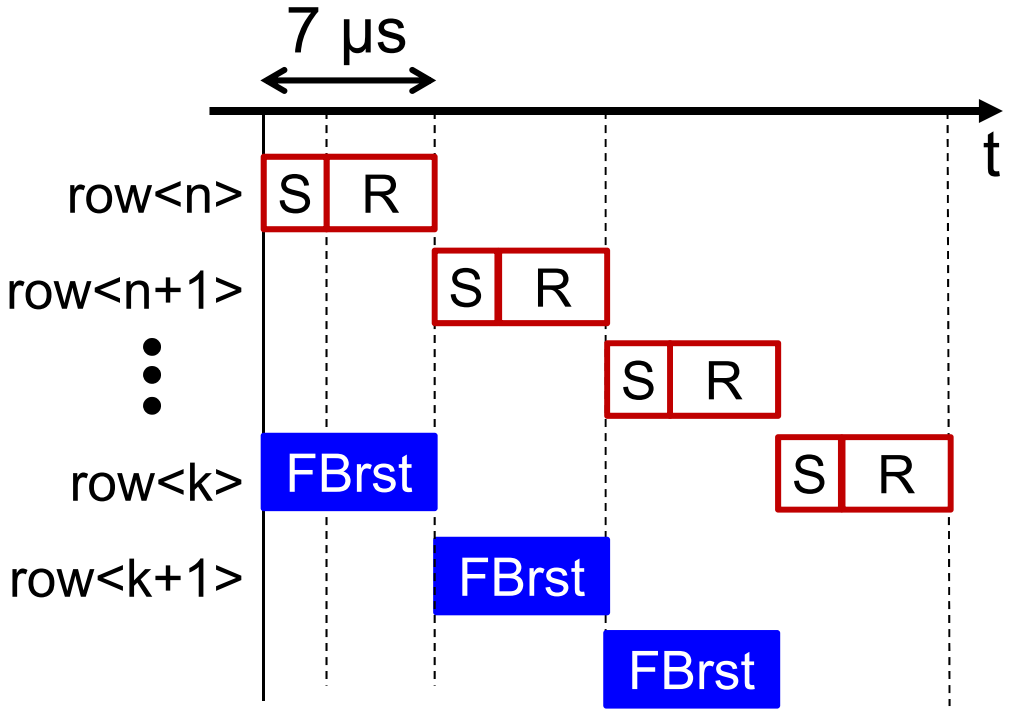
High Speed Reference Readout



Pixel-separated reference readout is executed for high speed read



H cycle can be shortened from 14 µs to 7 µs

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Captured Image

Both images are captured by fabricated OPF sensor

Rolling shutter mode

Global shutter mode

60fps w/ high speed readout

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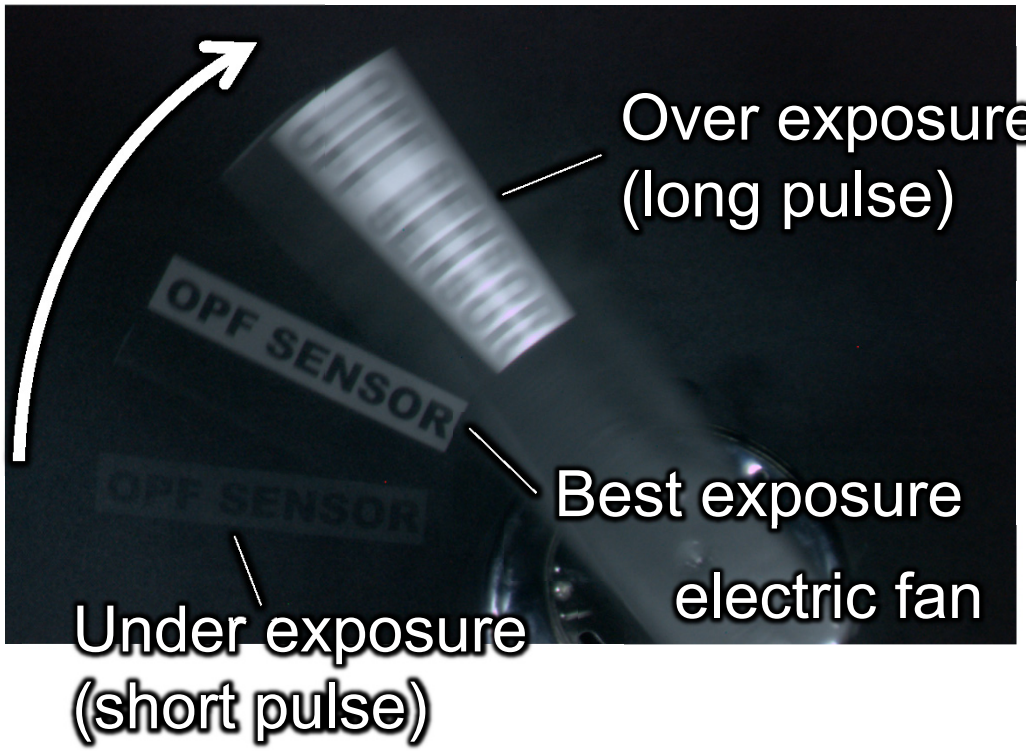
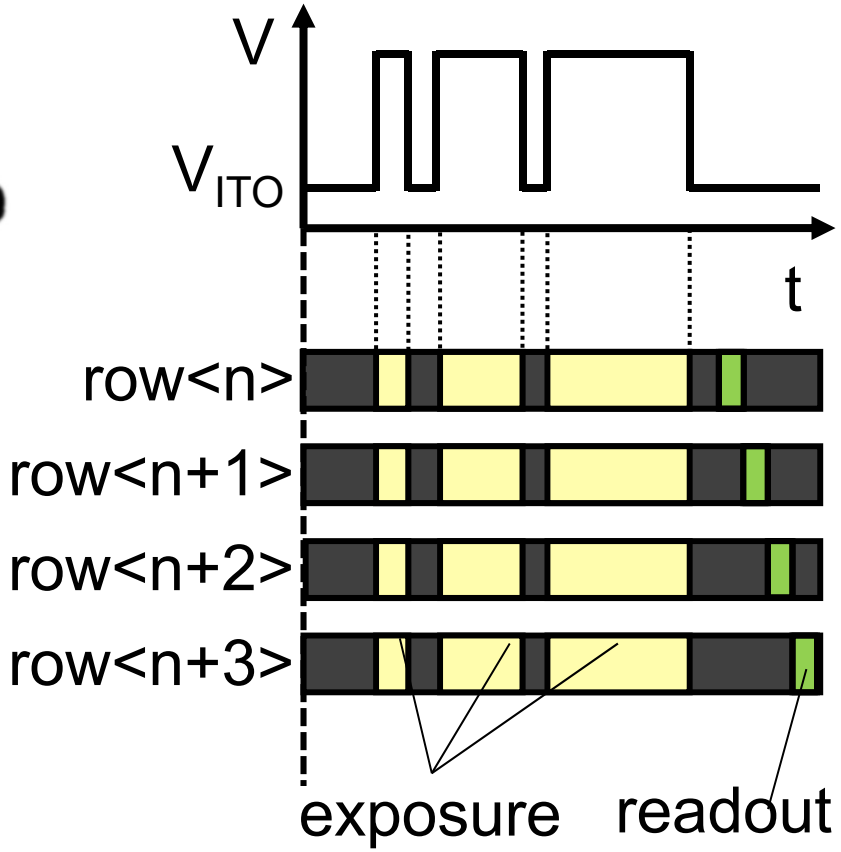
Multiple Exposure Image

Multiple exposure by variable pulse duty





Character recognition by choosing optimum exposure time

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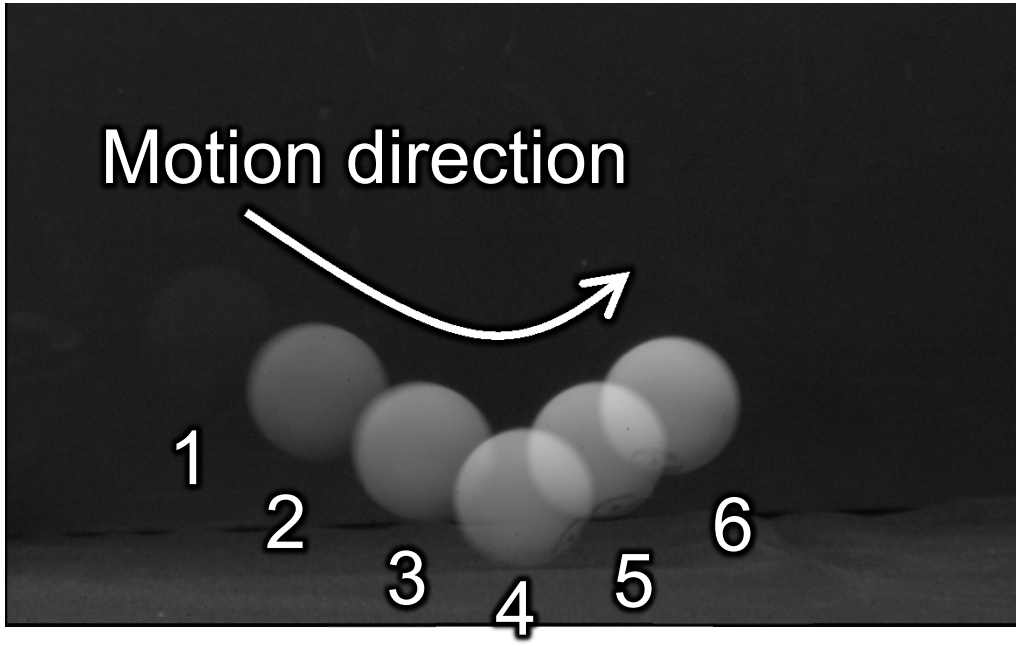
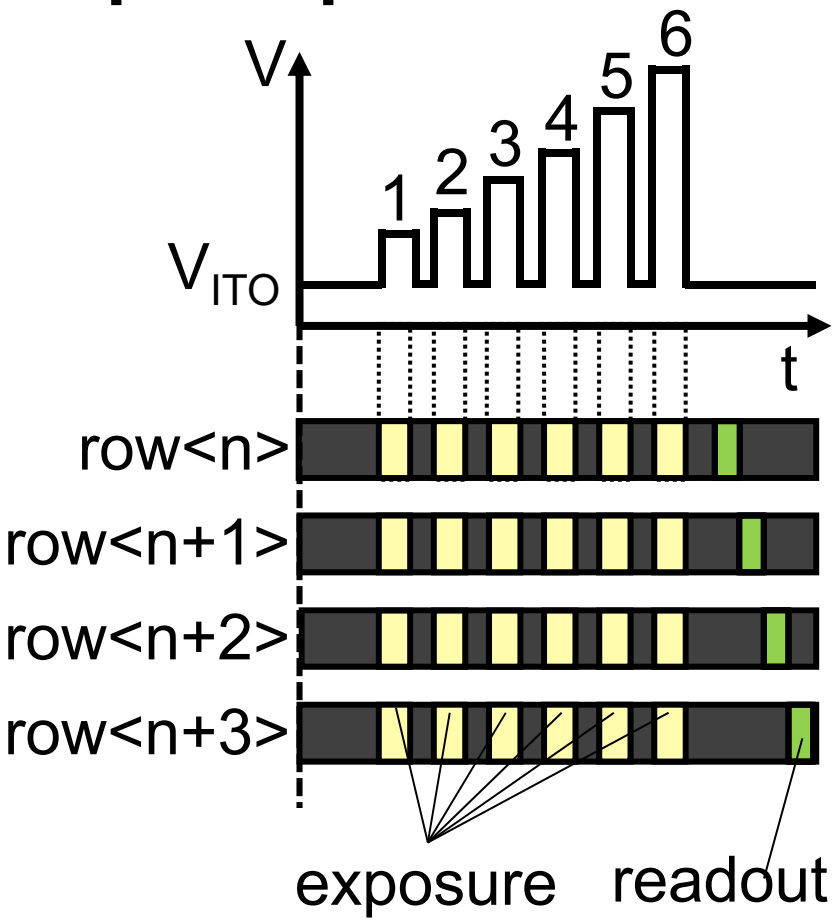
Multiple Exposure Image

"Variable sensitivity multiple exposure"





Motion direction can be detected by acquired signal level

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Performance Comparison

	This work	IEDM2015[2]	ISSCC2012[1]
Sensor type	OPF CMOS	3D stacked	CMOS
Pixel count	1,920 x 1,080	4,608 x 3,480	10M (single) 5M (dual)
Pixel size [μm^2]	3.0 x 3.0	3.8 x 3.8	5.86 x 5.86
Random noise [e-]	4.4	-	4.8
PLS [dB]	-106dB	-180dB	-100dB
Saturation [e-]	51k (normal) 210k (SAT-on)	35k	32.2k (single) 67.7k (dual)
Saturation /pixel area [e-/μm^2]	5,678 (normal) 23,333 (SAT-on)	2,423	938 (single) 1,972 (dual)
VSME function	○	-	-

VSME: Variable sensitivity multiple exposure

Highest saturation signal GS pixel is achieved.

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Summary

We successfully developed OPF image sensor

- 210ke- global shutter operation
- Global sensitivity controlled multiple exposure

New Imaging & Sensing Applications
will be realized by OPF image sensor
with High saturation, High functional GS operation!

Acknowledgement

The authors would like to thank FUJIFILM Corporation for supplying organic film materials and technical supports.

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105 x 65 mm^2 391 Mpixel CMOS Image Sensor with >78 dB Dynamic Range for Airborne Mapping Applications

Jan Bogaerts, Raf Lafaille, Marc Borremans, Jia Guo, Bart Ceulemans, Guy Meynants, Navid Sarhangnejad, Gavril Arsinte, Victor Statescu, Sonja van der Groen

CMOSIS, AMS CIS Business Line

ISSCC 2016

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Outline

- Application background
- Sensor architecture
- Sensor timing diagram
- Signal readout path
- Noise, FWC and Dynamic Range
- Summary characteristics
- Example test images

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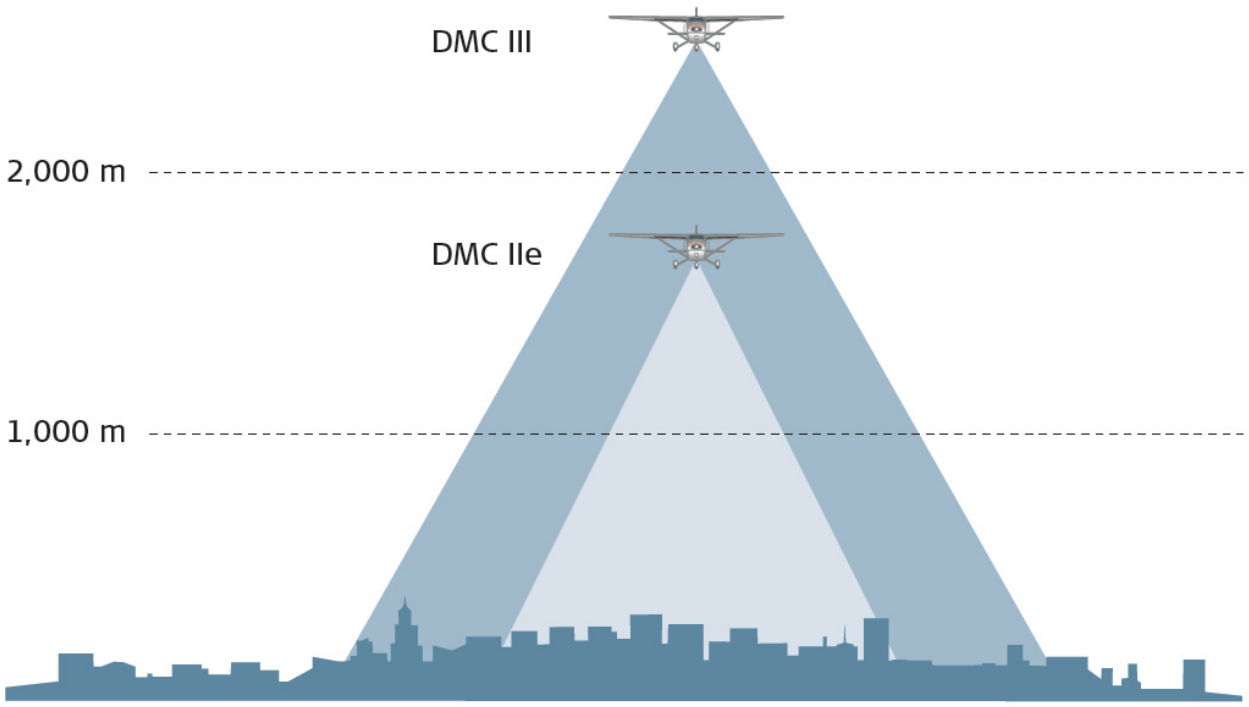
Mapping application



Higher sensor resolution: time & cost reduction

→ higher flight altitude for same GSD*

→ better GSD for similar flight altitude

*GSD = ground sampling distance

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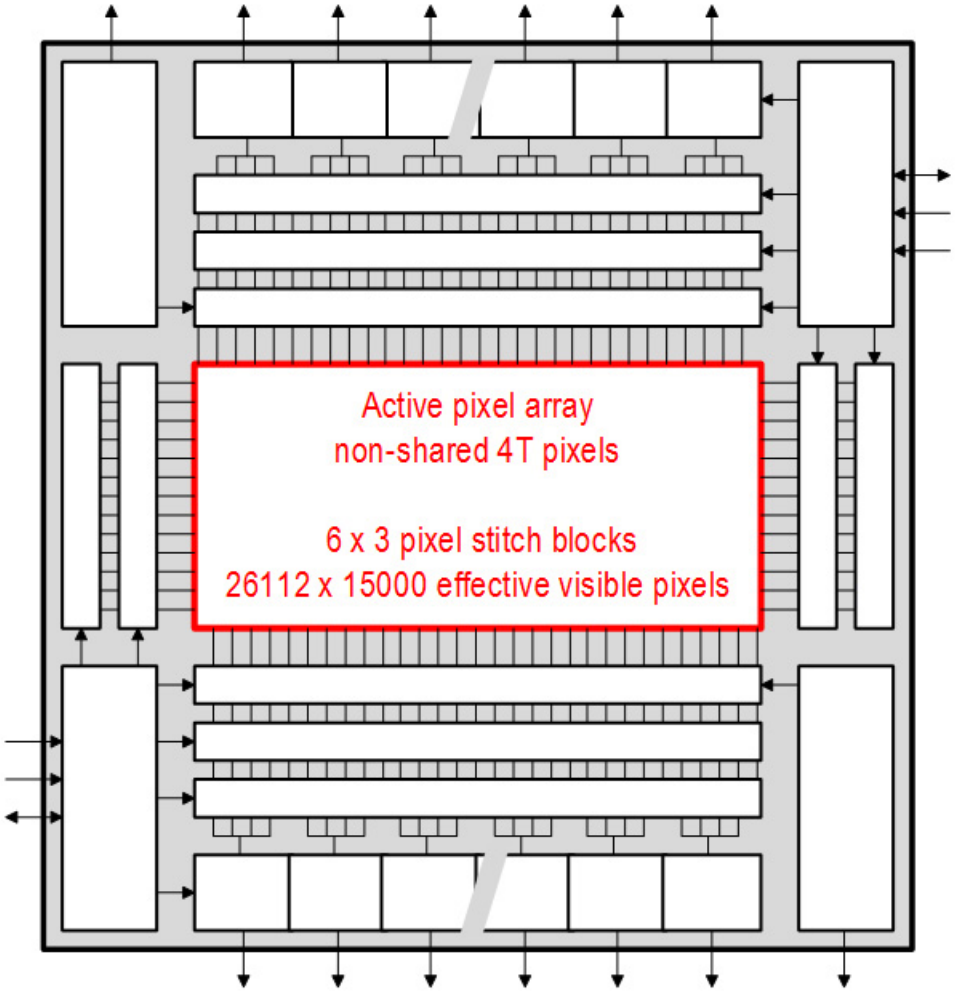
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm
Pixel pitch:
3.9 µm
Sensor size > reticle size
→ 2D stitching

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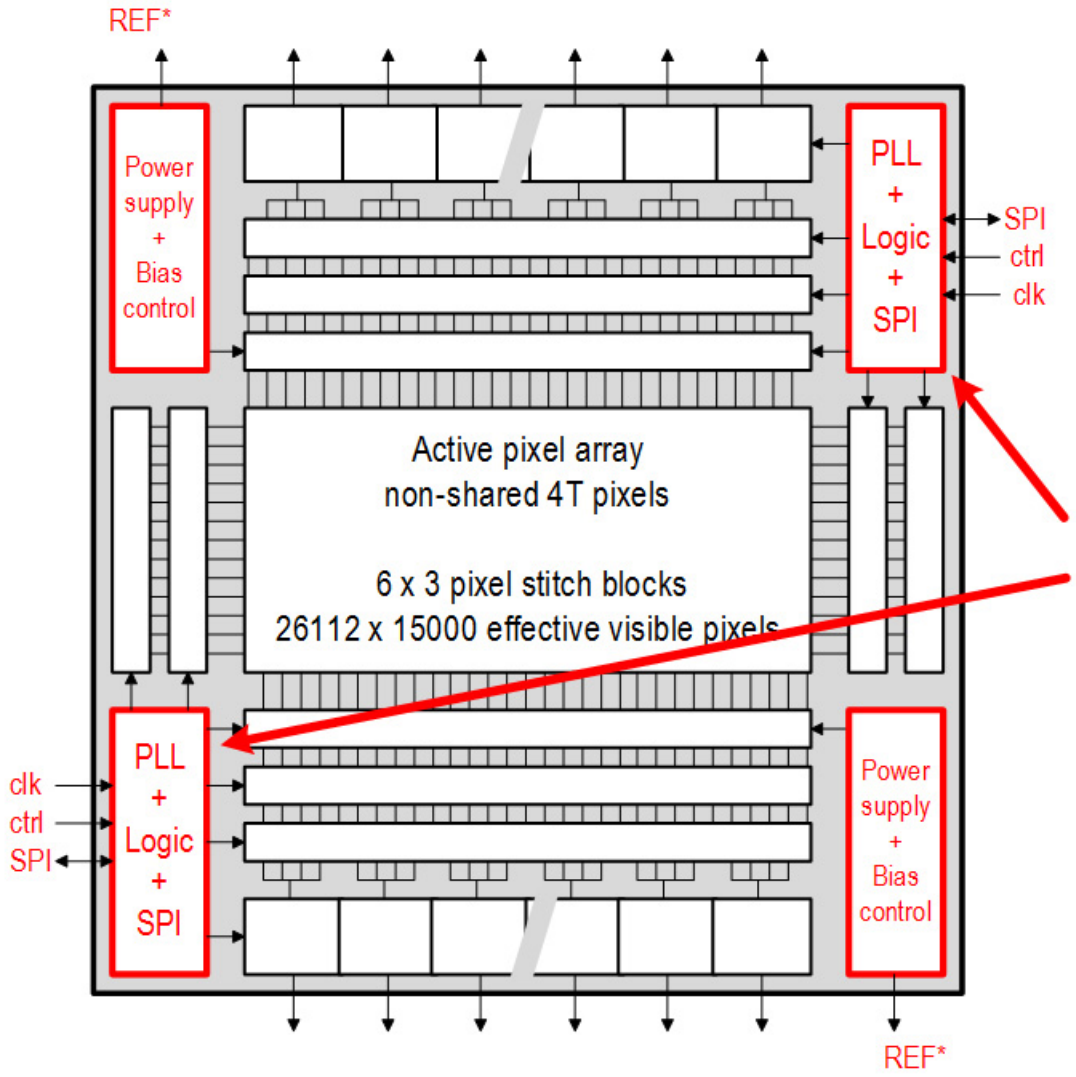
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm
Pixel pitch:
3.9 µm
Sensor size > reticle size
→ 2D stitching

2 logic control blocks

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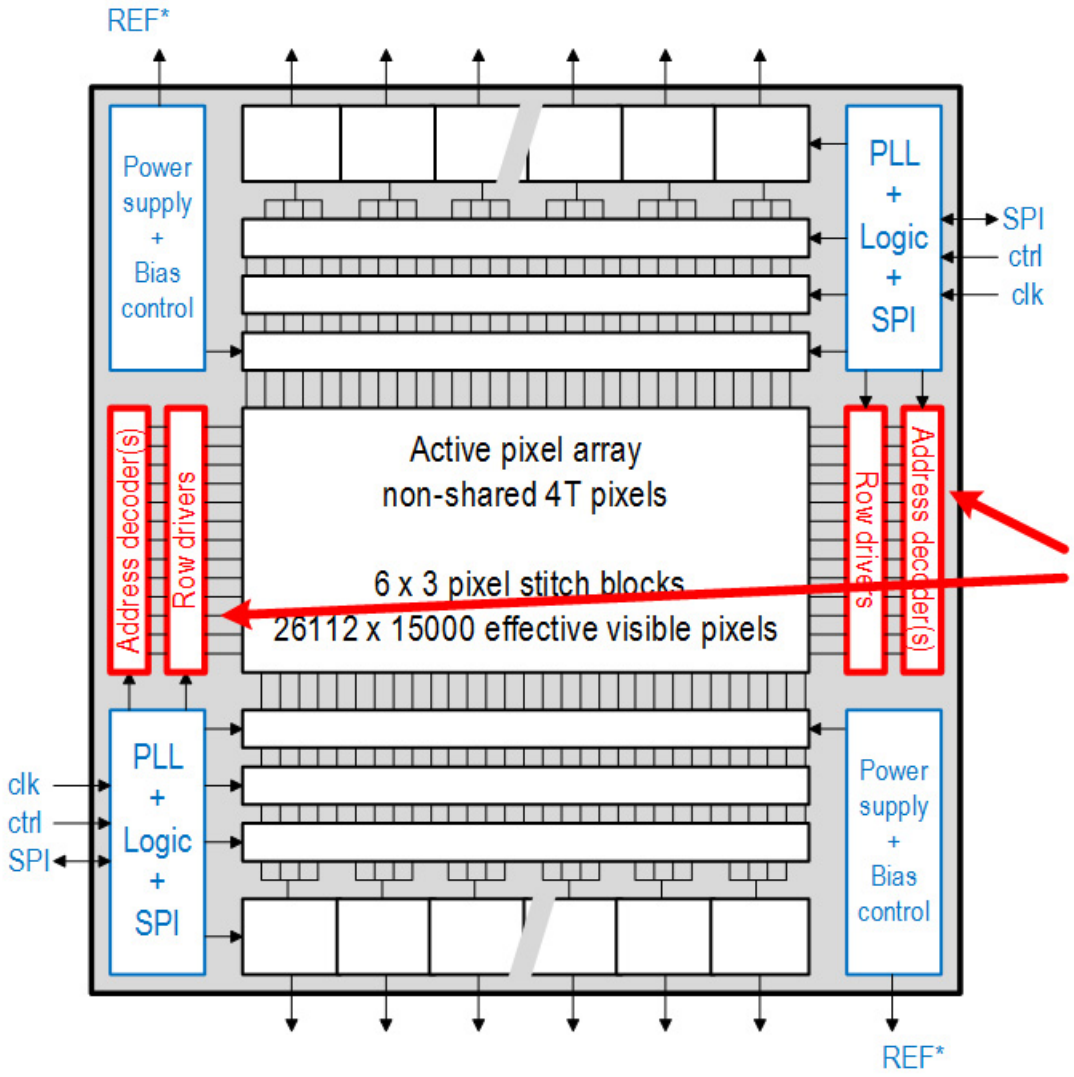
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm
Pixel pitch:
3.9 µm
Sensor size > reticle size
→ 2D stitching

Y address decoders & drivers

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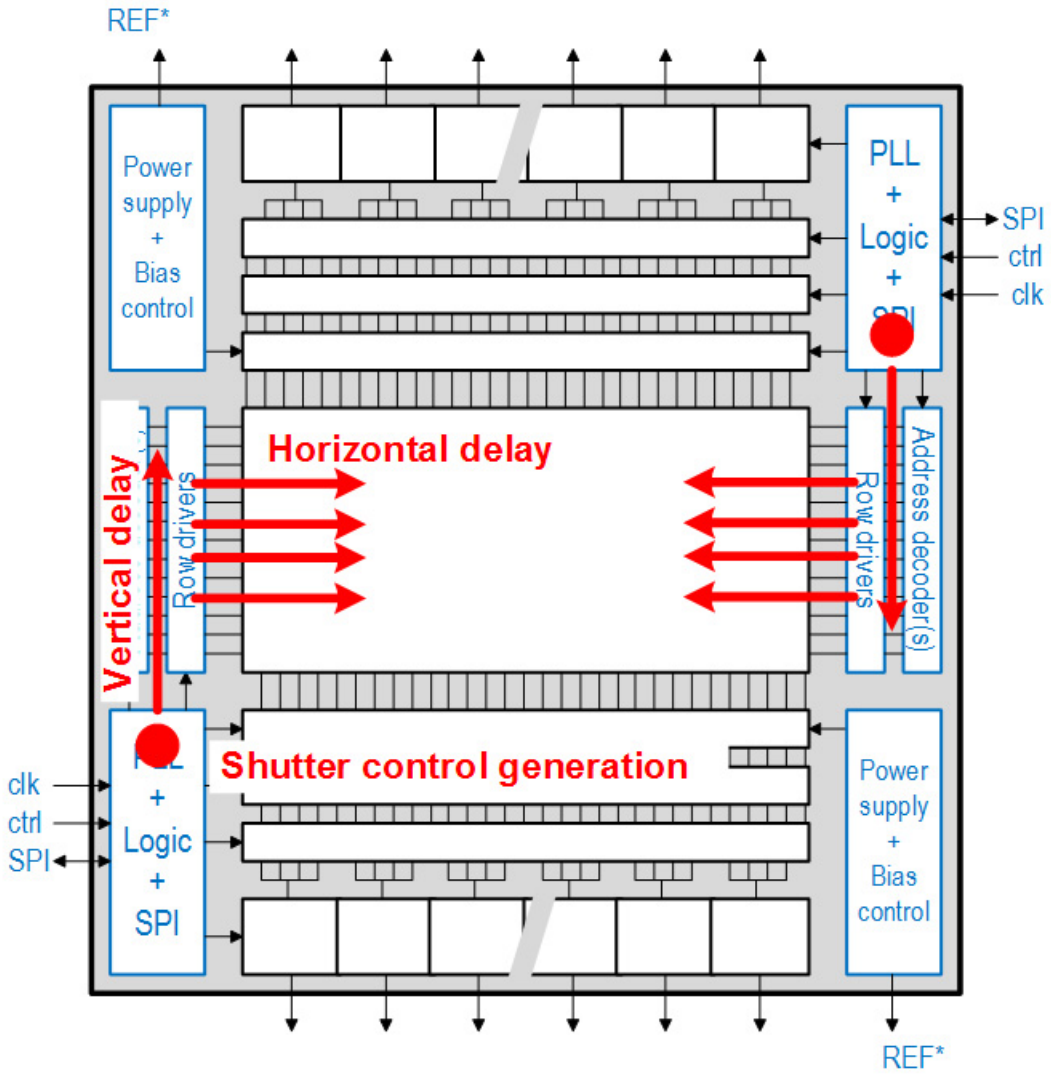
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm

Pixel pitch:
3.9 µm

Sensor size > reticle size
→ 2D stitching

Global shutter control:
uniformity better than 2.5 µs

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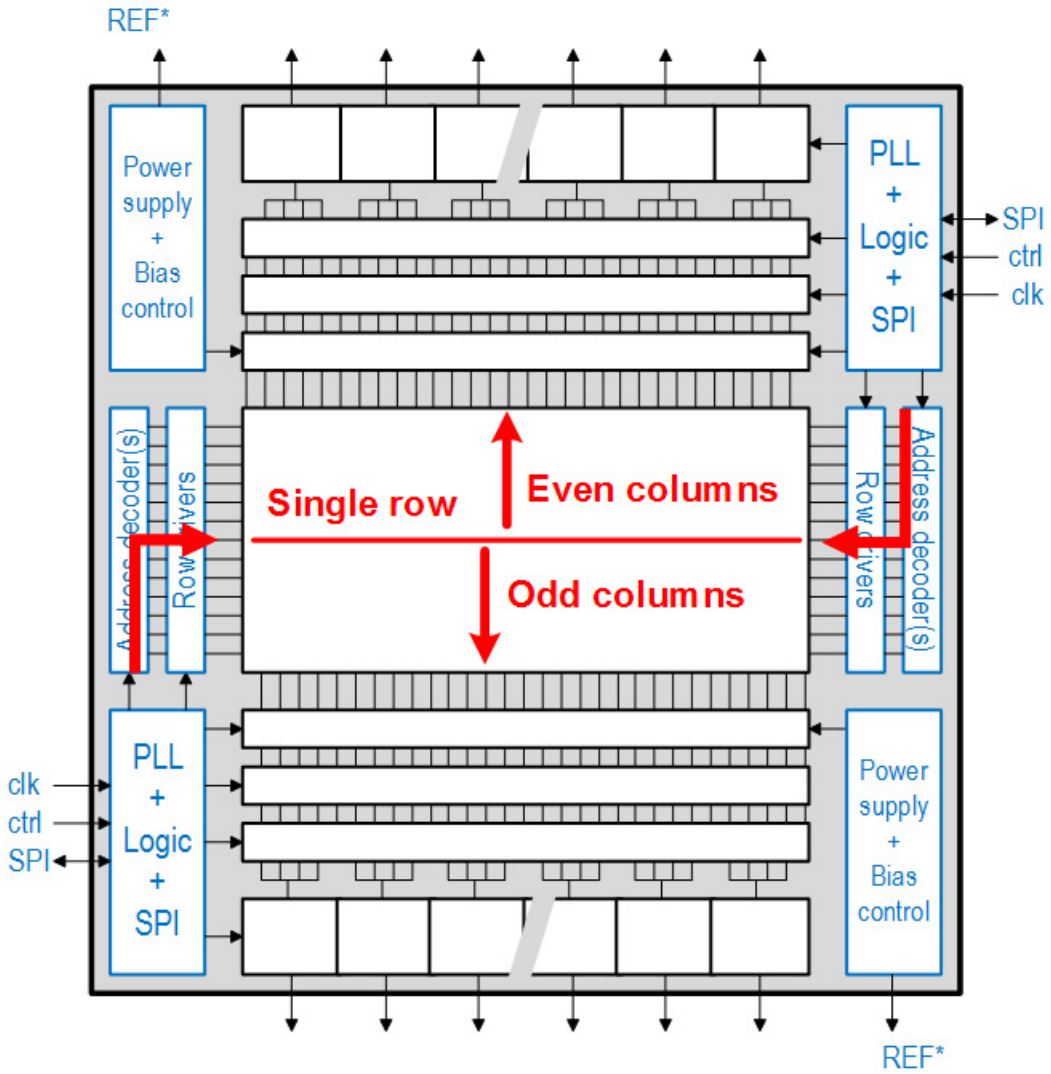
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm

Pixel pitch:
3.9 µm

Sensor size > reticle size
→ 2D stitching

Global shutter control:
uniformity better than 2.5 µs

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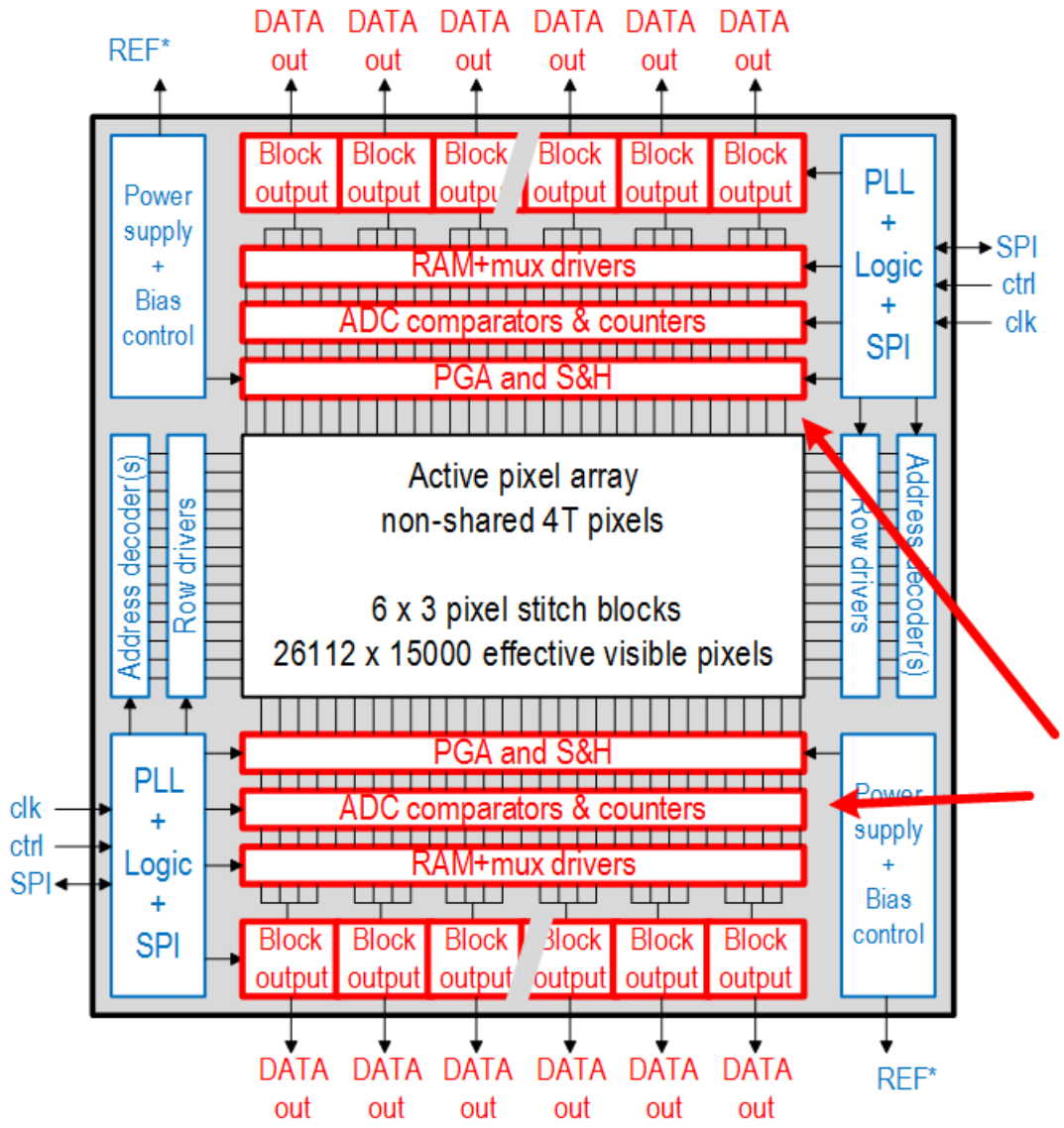
Sensor architecture



Process technology:
1P4M, FE 90nm / BE 65 nm

Pixel pitch:
3.9 µm

Sensor size > reticle size
→ 2D stitching

Global shutter control:
uniformity better than 2.5 µs

Each side: 7.8 µm pitch
PGA and 2x S&H banks
column ADC
SRAM & 12 output channels

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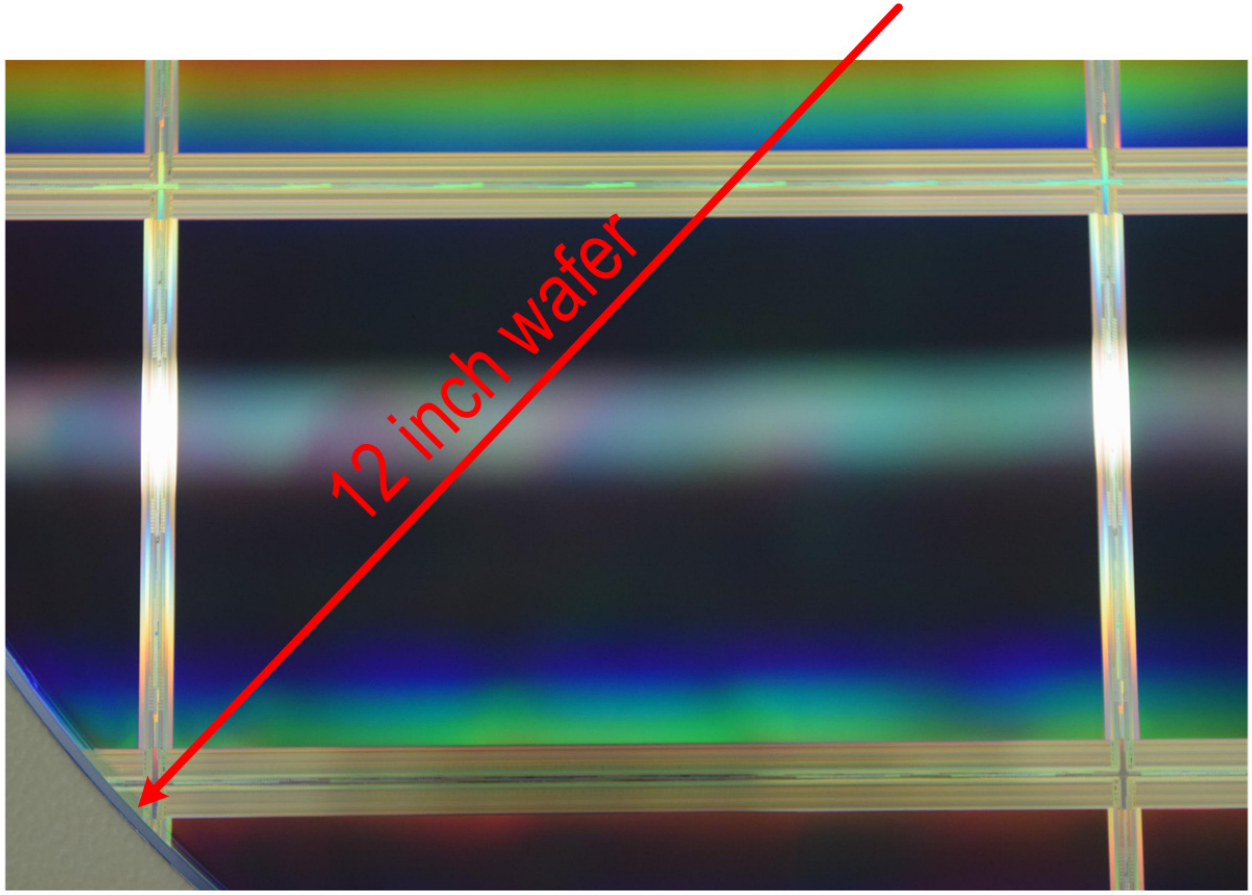
Sensor photograph



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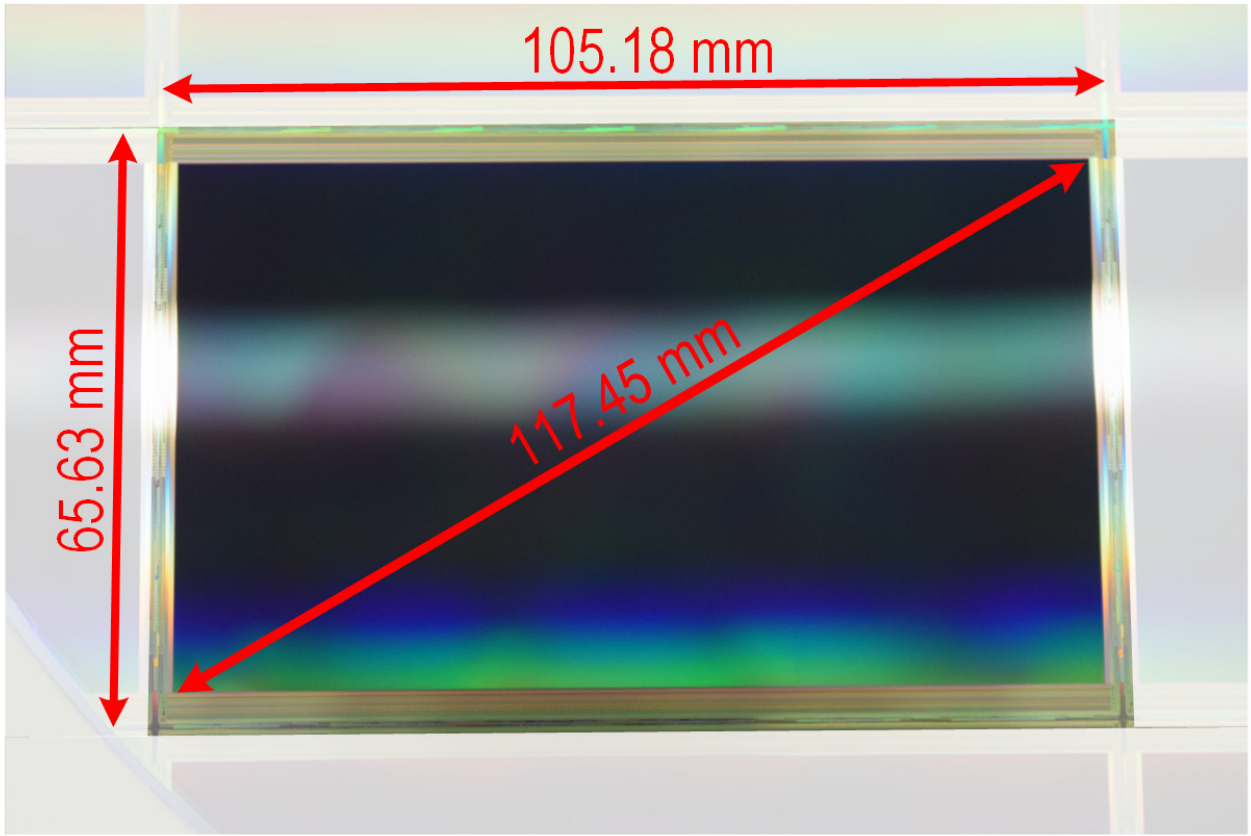
Sensor photograph



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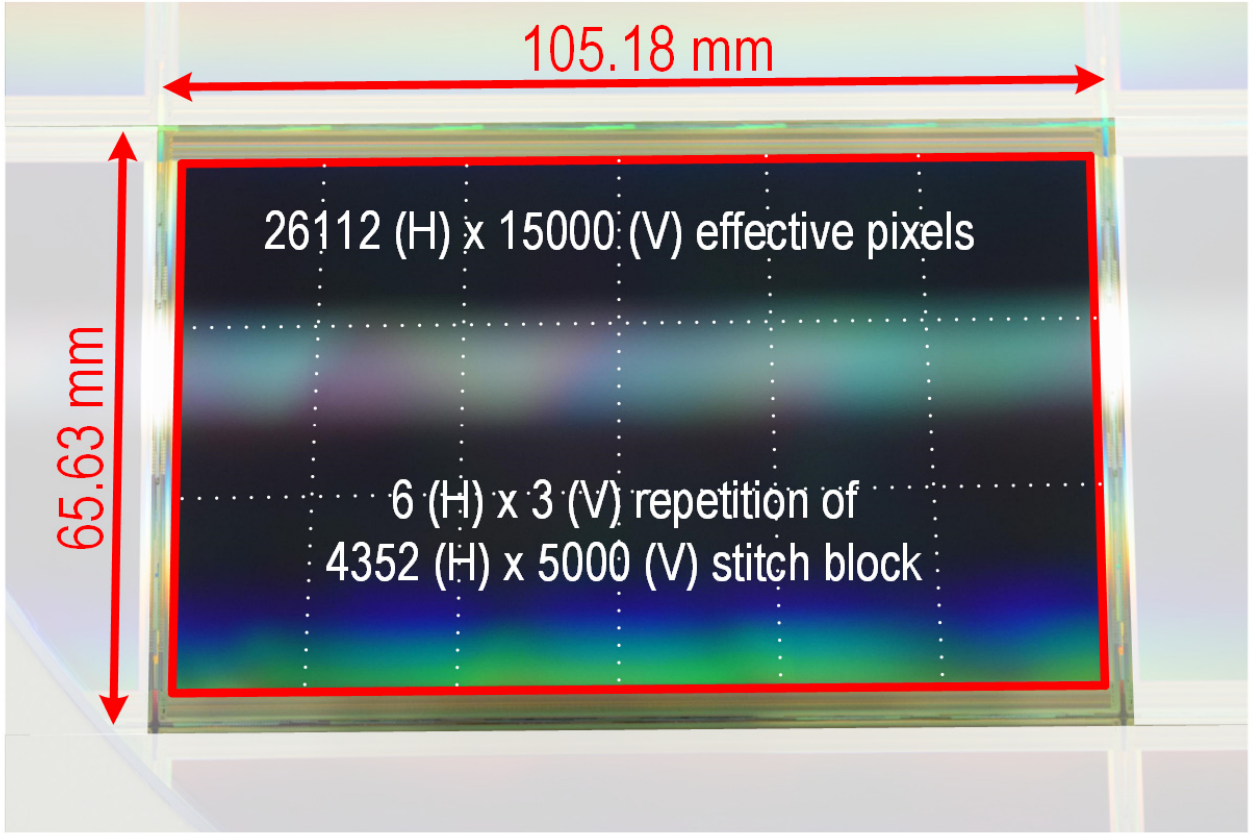
Sensor photograph



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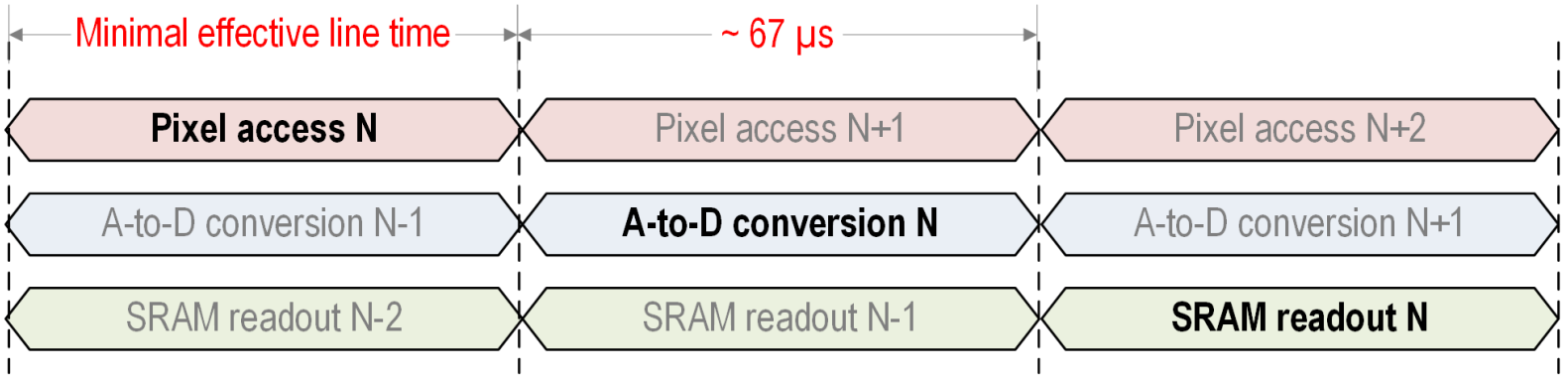
Sensor timing diagram

Frame rate specification: 1 fps



Pipelining of 3 processes

Ramp A-to-D convertors with dual counters per column

Counter data written serially into SRAM

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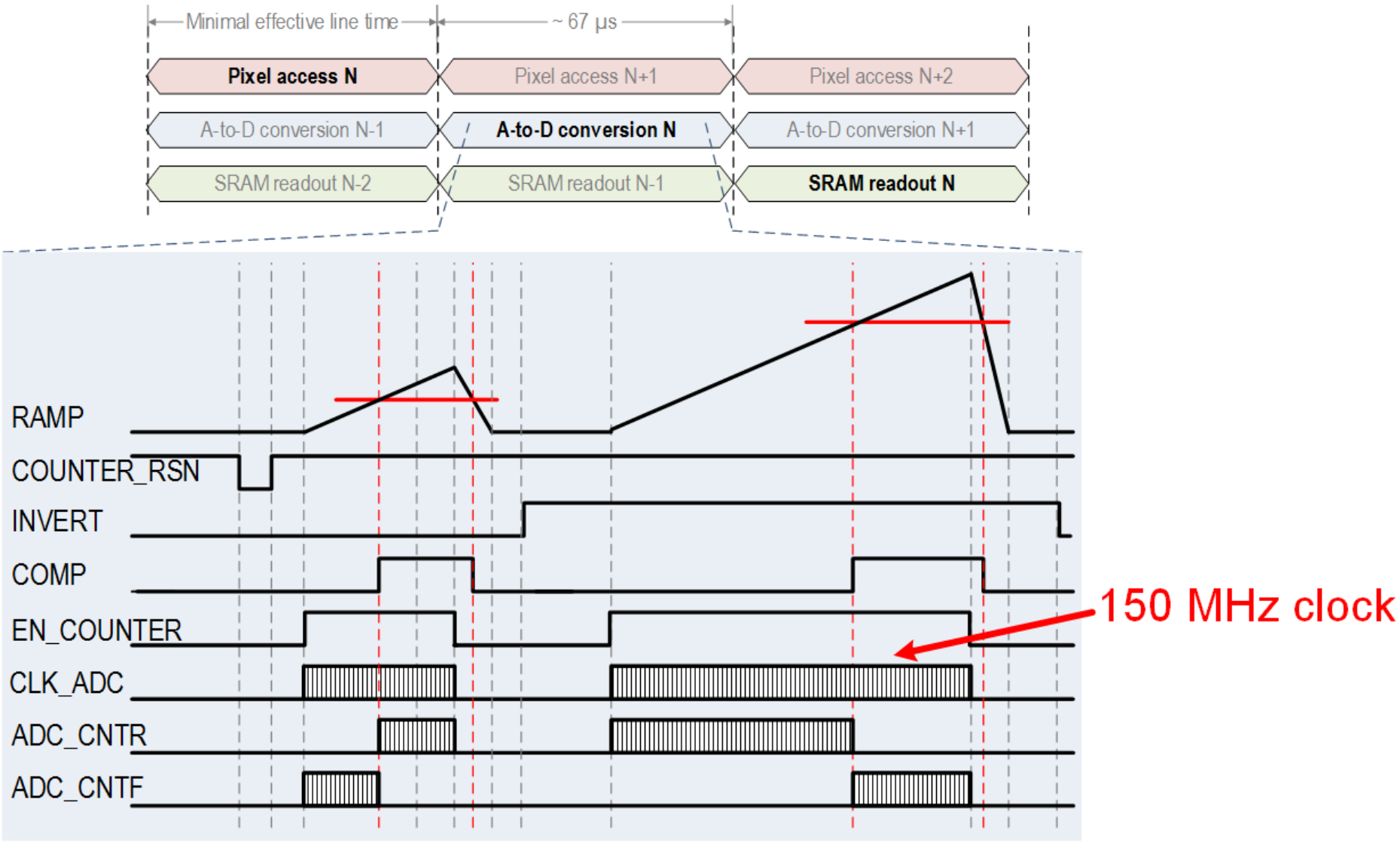
Sensor timing diagram



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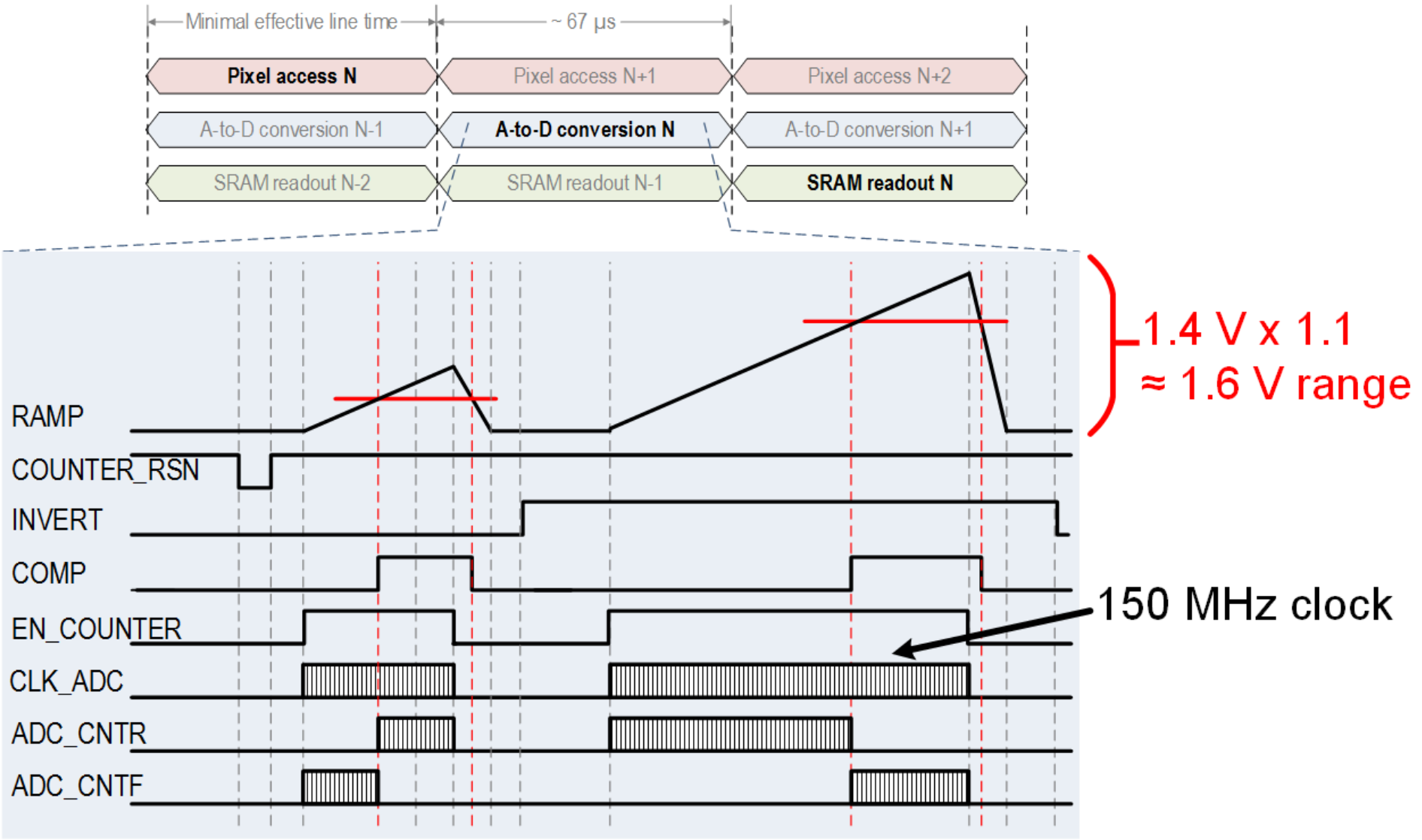
Sensor timing diagram



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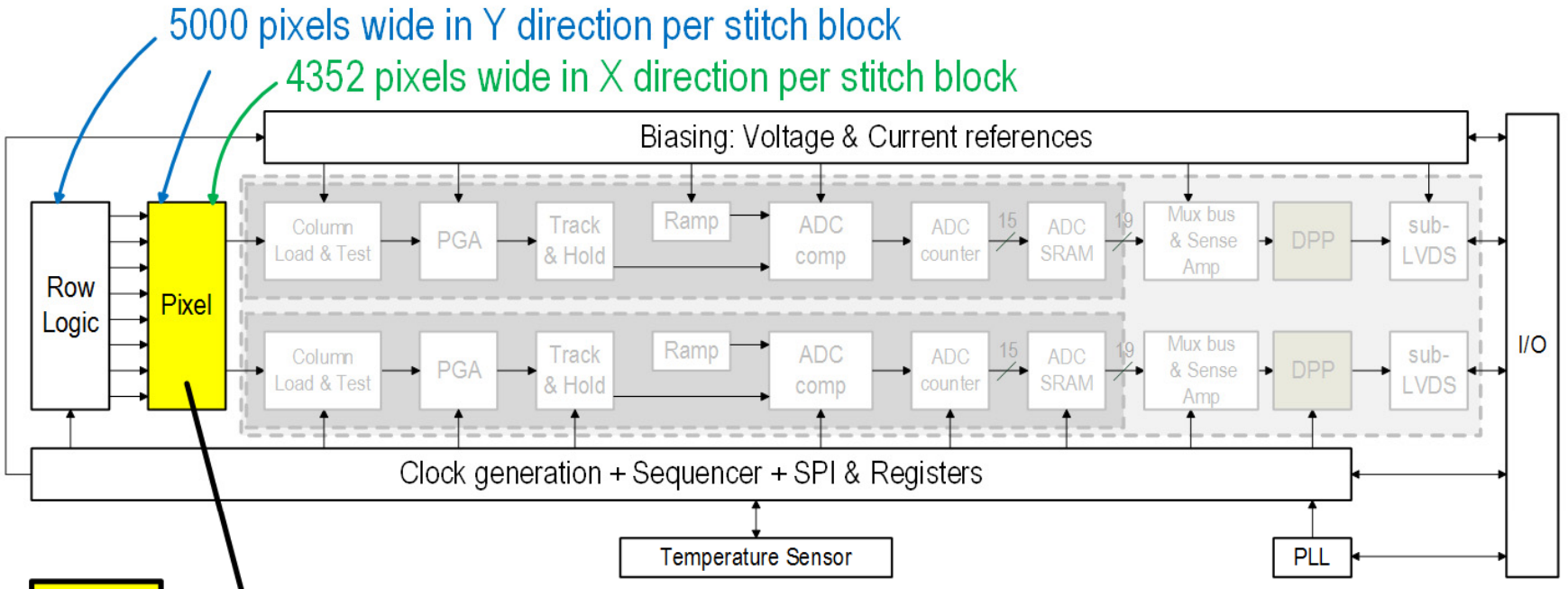
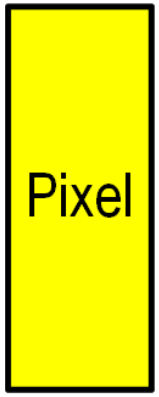
Signal readout path





Effective pixel array:

6 (H) x 3 (V) stitch blocks

4352 (H) x 5000 (V) pixels per block

} > 391 Mpixels

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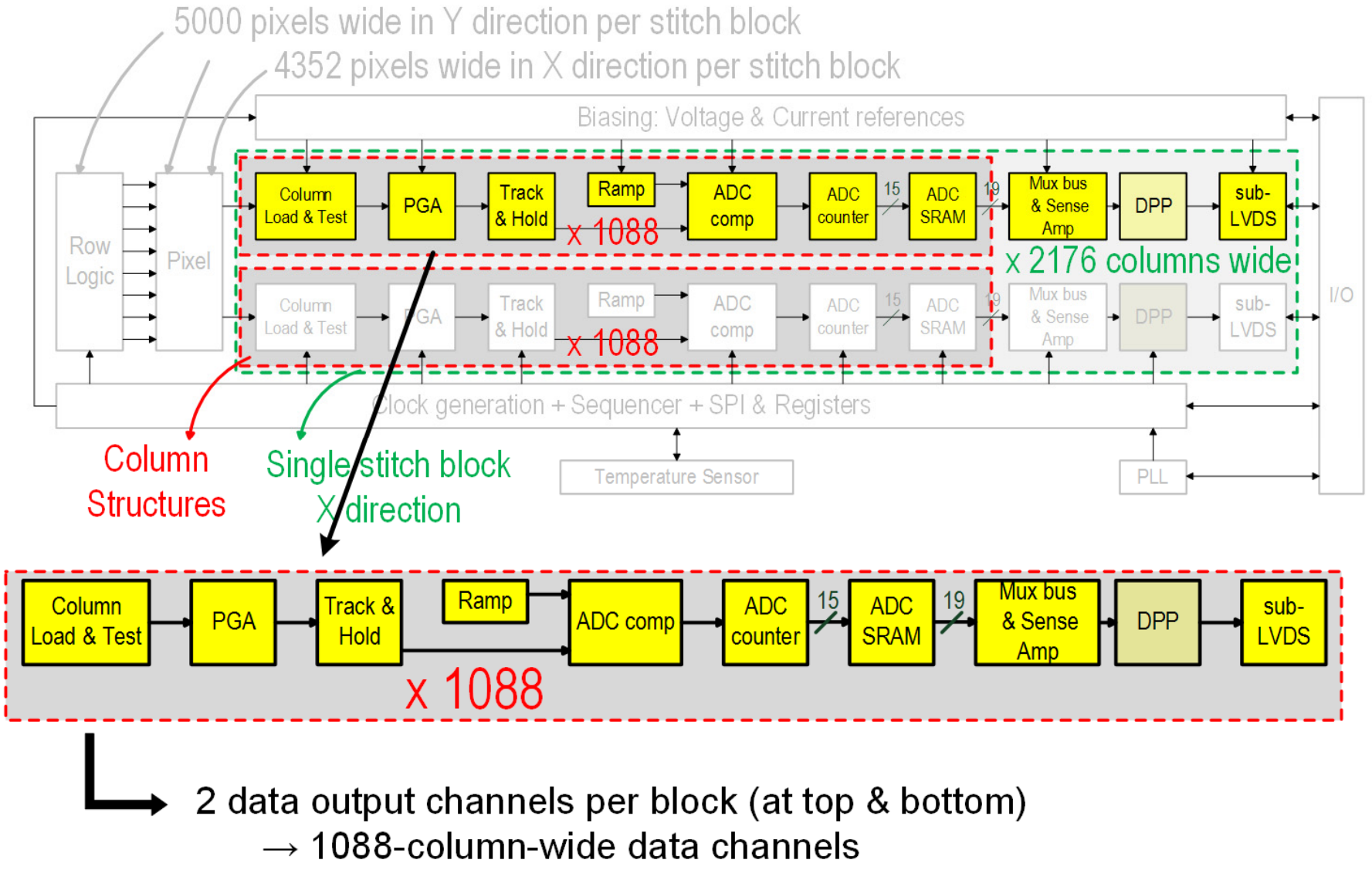
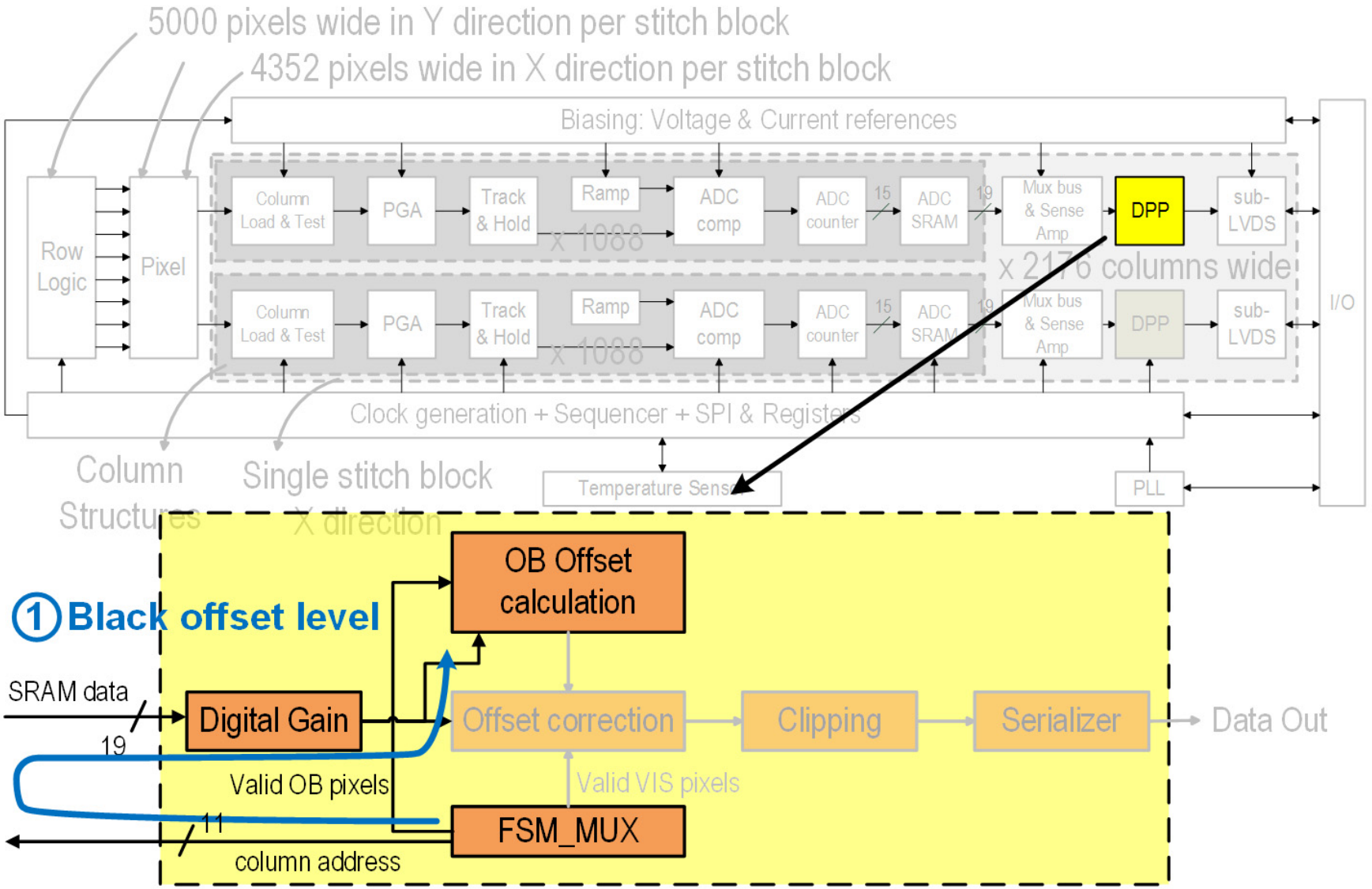
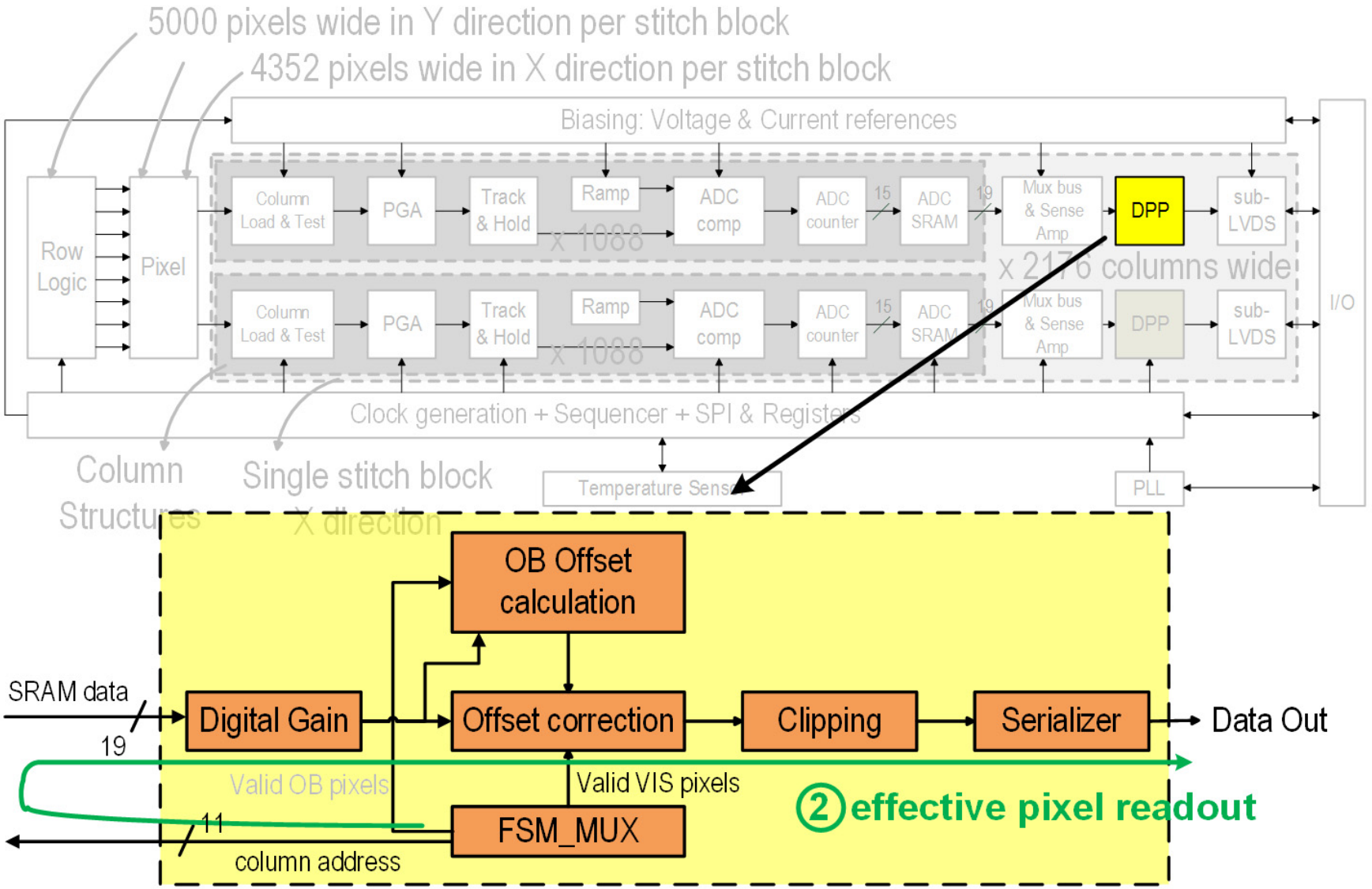
Signal readout path



Signal readout path



Signal readout path



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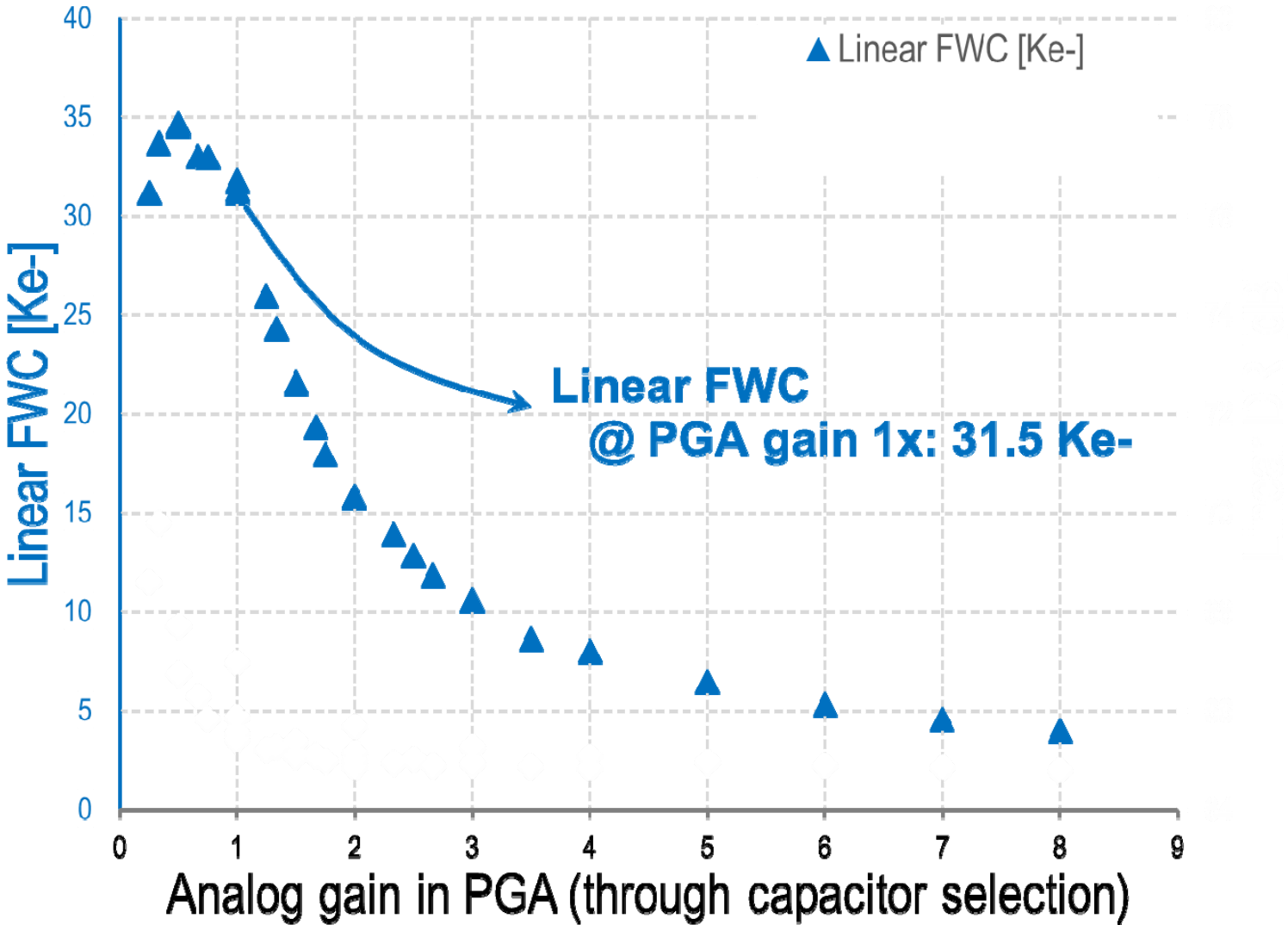
Noise, FWC and dynamic range



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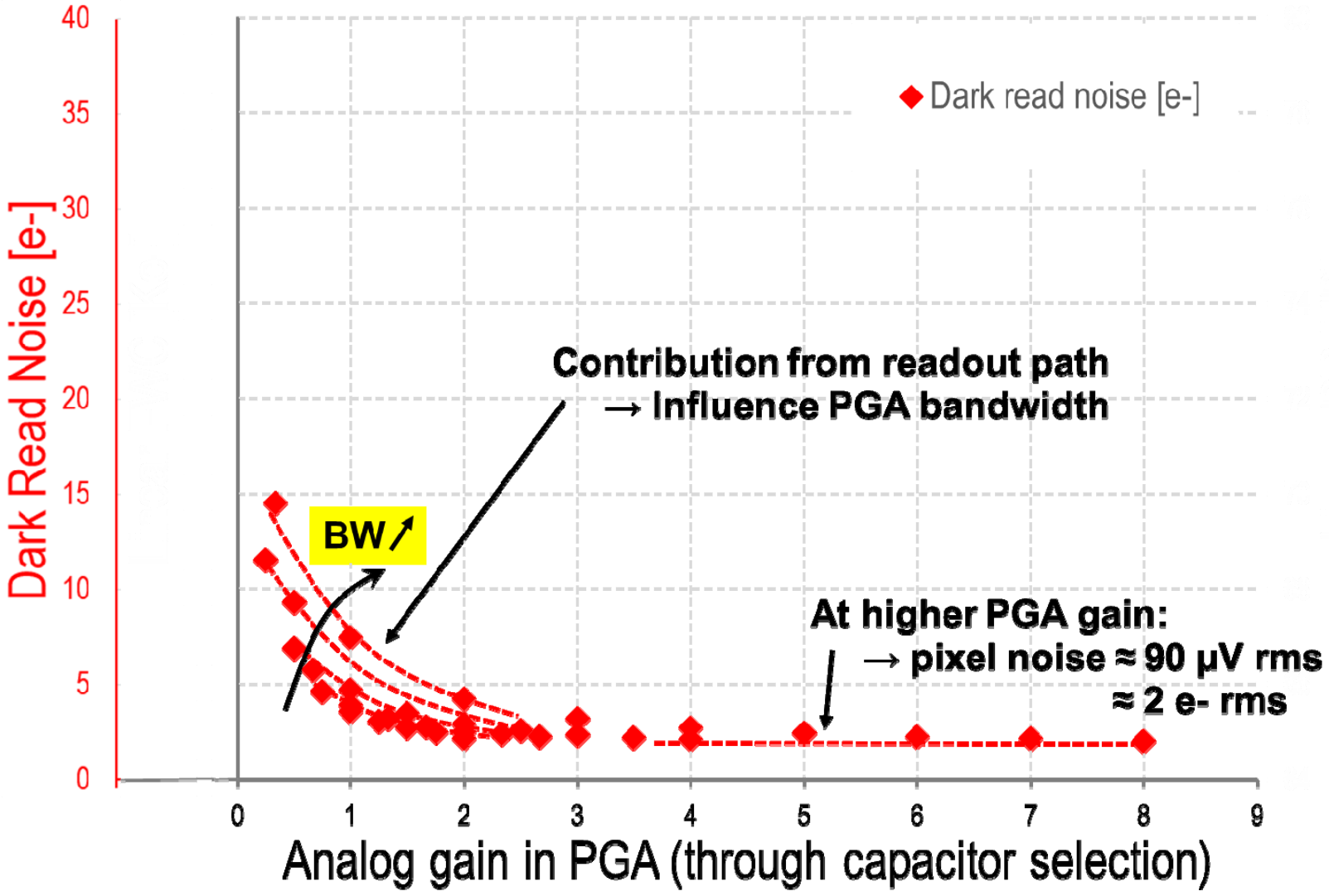
Noise, FWC and dynamic range



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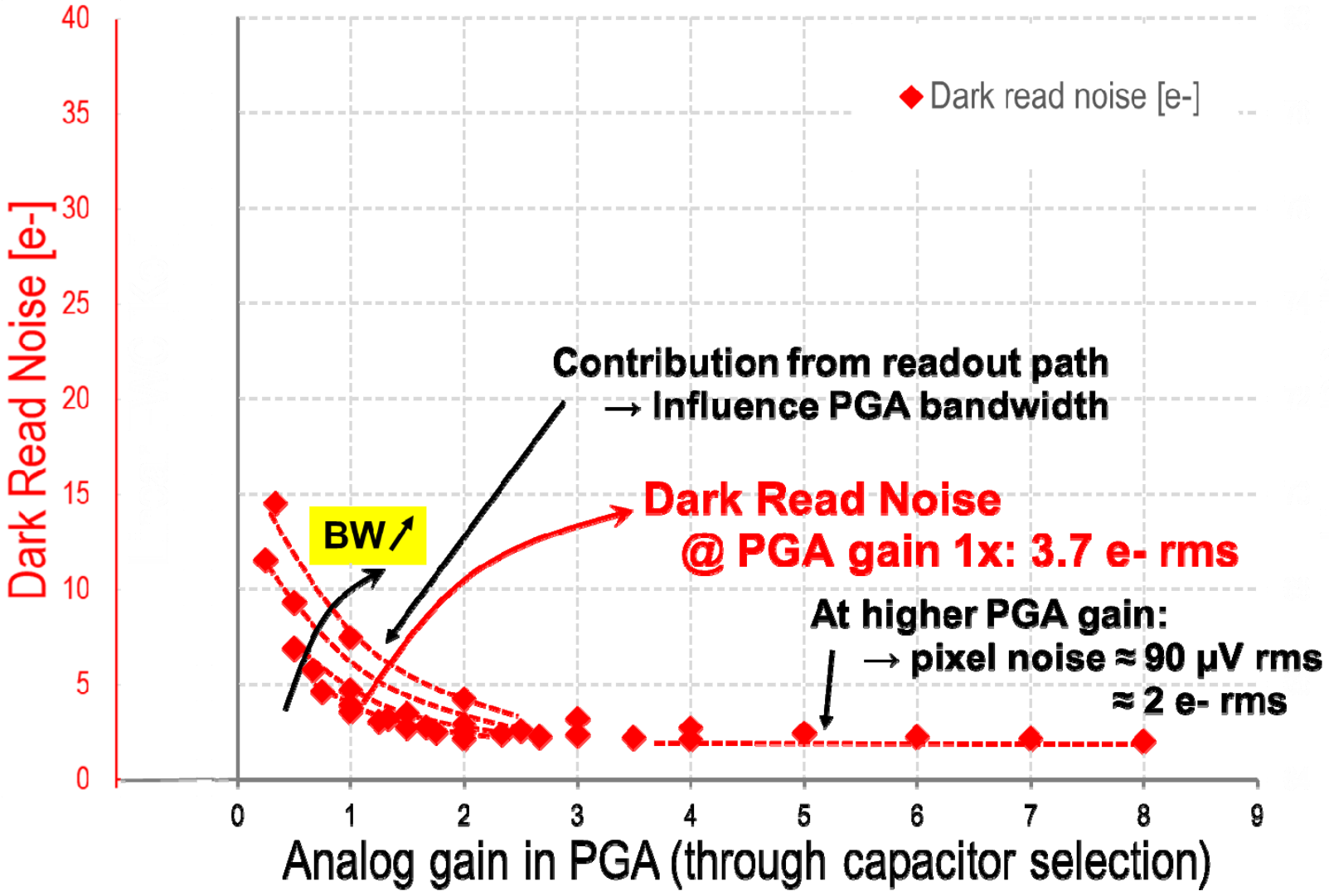
Noise, FWC and dynamic range



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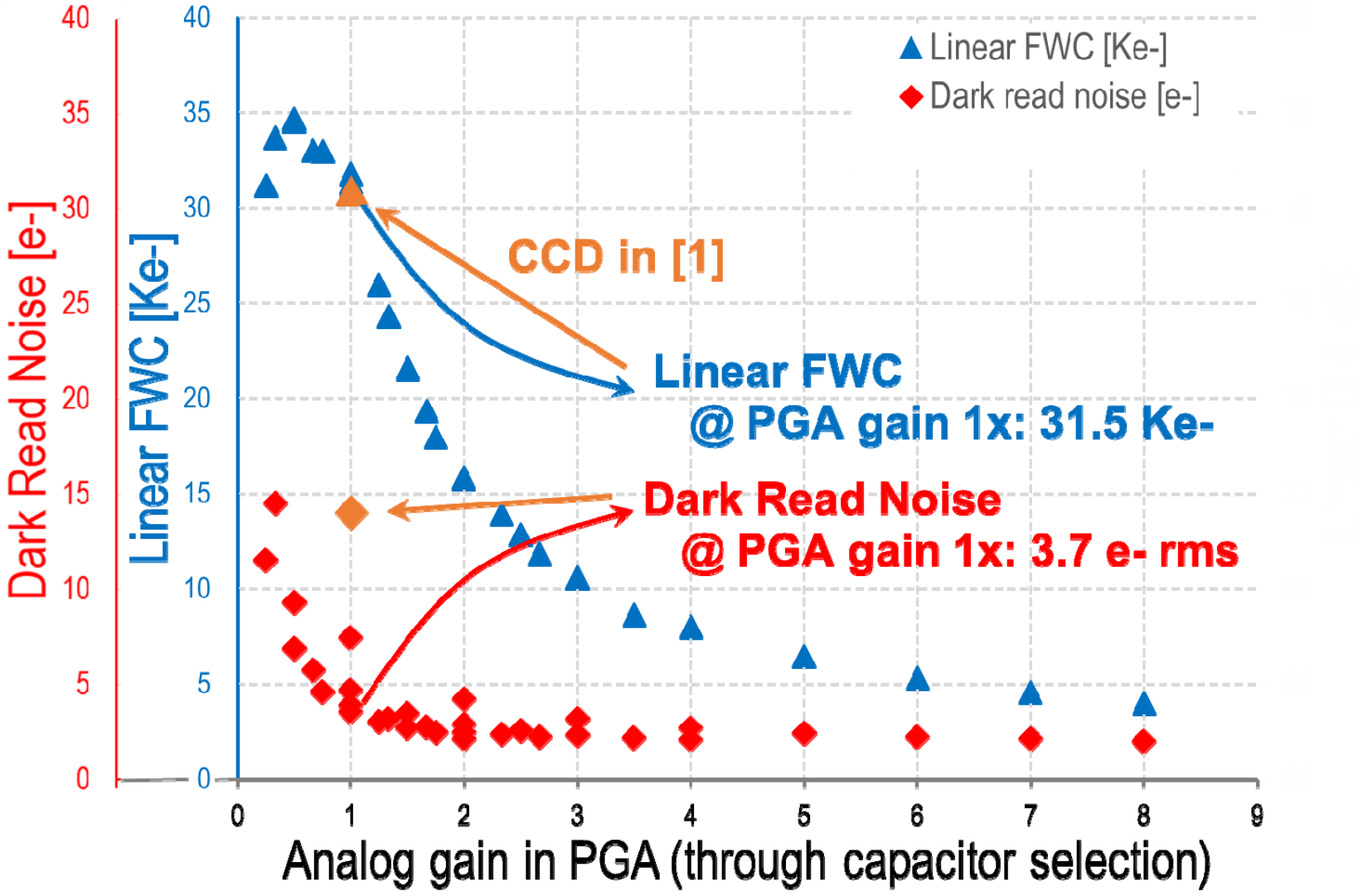

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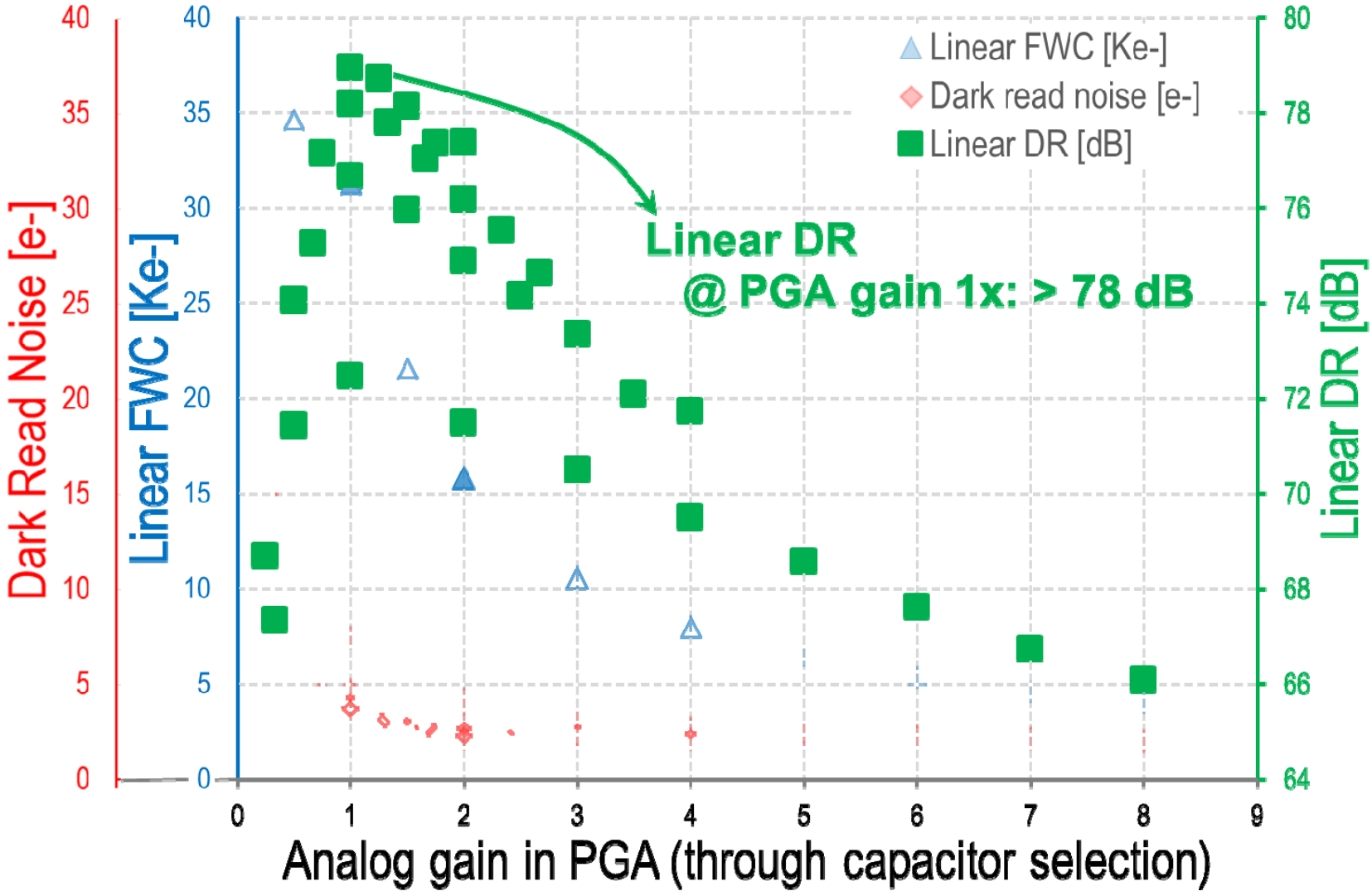

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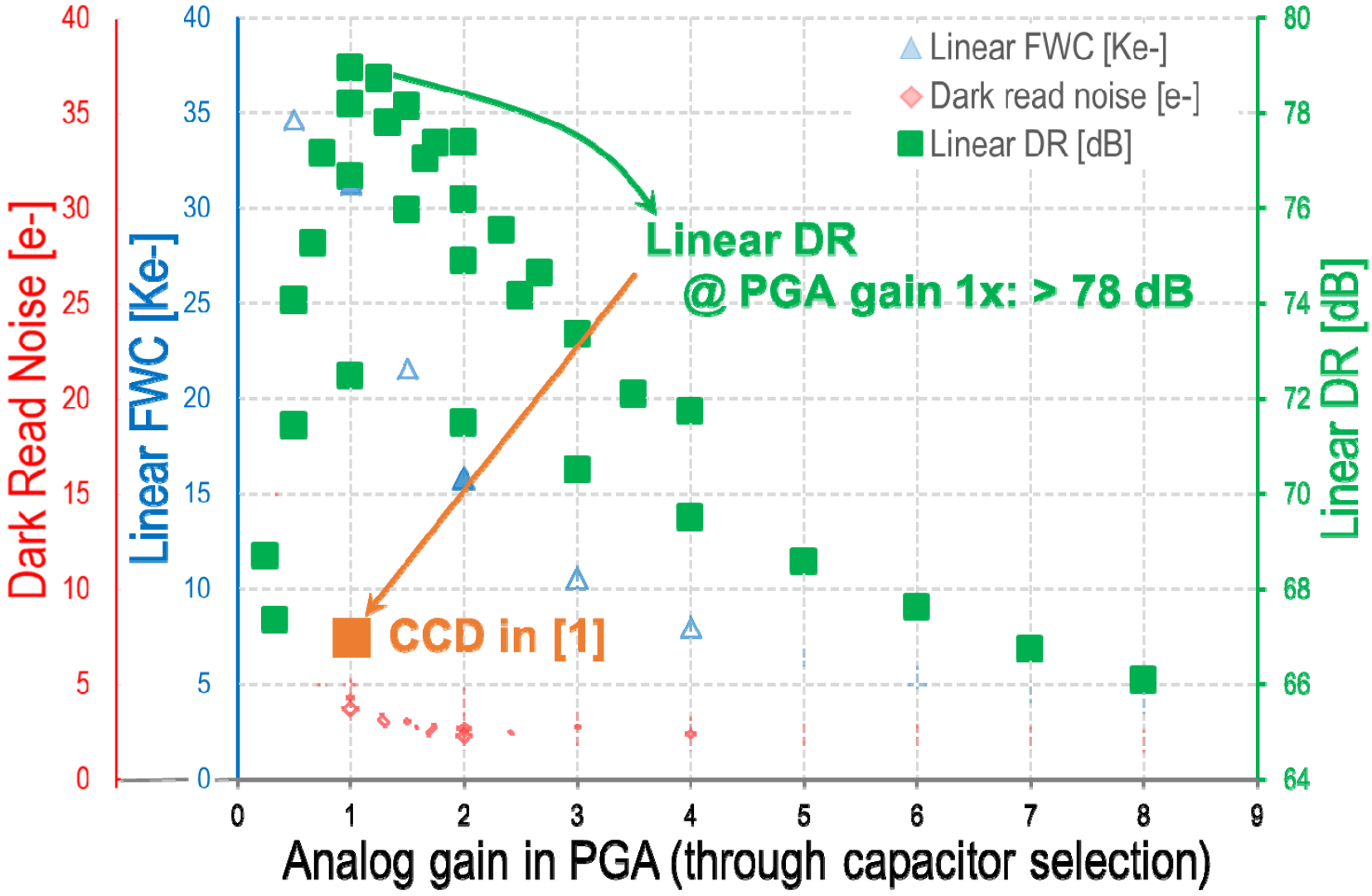
Noise, FWC and dynamic range



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Summary characteristics

		This work	[1]
Technology	90 nm FE, 65 nm BE, 1P4M, 12 inch wafers		CCD
Pixel size	3.9 µm pitch		5.6 µm pitch
Number of pixels	Total	26456 (H) x 15072 (V)	
	Effective	26112 (H) x 15000 (V)	17216 (H) x 14656 (V)
Frame rate	1 fps		1 fps
Clock input	6-12 MHz		27 MHz
Output data	Type	24 effective data + 4 OB + 2 clock LVDS lanes @ 300 Mbps (DDR)	16 analog channels
	Total Rate	5.474 Gbps from effective pixels	
Linear FWC	31.5 Kelectrons @ PGA 1x and 1 % linearity		~ 31.3 Kelectrons (calc.)
Temporal noise	3.7 e- @ PGA 1x, 2 e- @ PGA 4x		14 e-
Dynamic range	> 78 dB @ PGA 1x, > 71 dB @ PGA 4x		67 dB
FPN	8.8 e- @ PGA 1x, short exposure time		
PRNU	1 % rms, stitch difference 0.5 %		
QE	75 % peak (mono, no CFA, with micro lens)		35-40 % peak (mono) (est.)
Angular response	> 80 % @ 18 °		
Dark current	95 e-/s @ 60 °C		
Power consumption	1750 mW @ 1 fps full resolution 14-bit		

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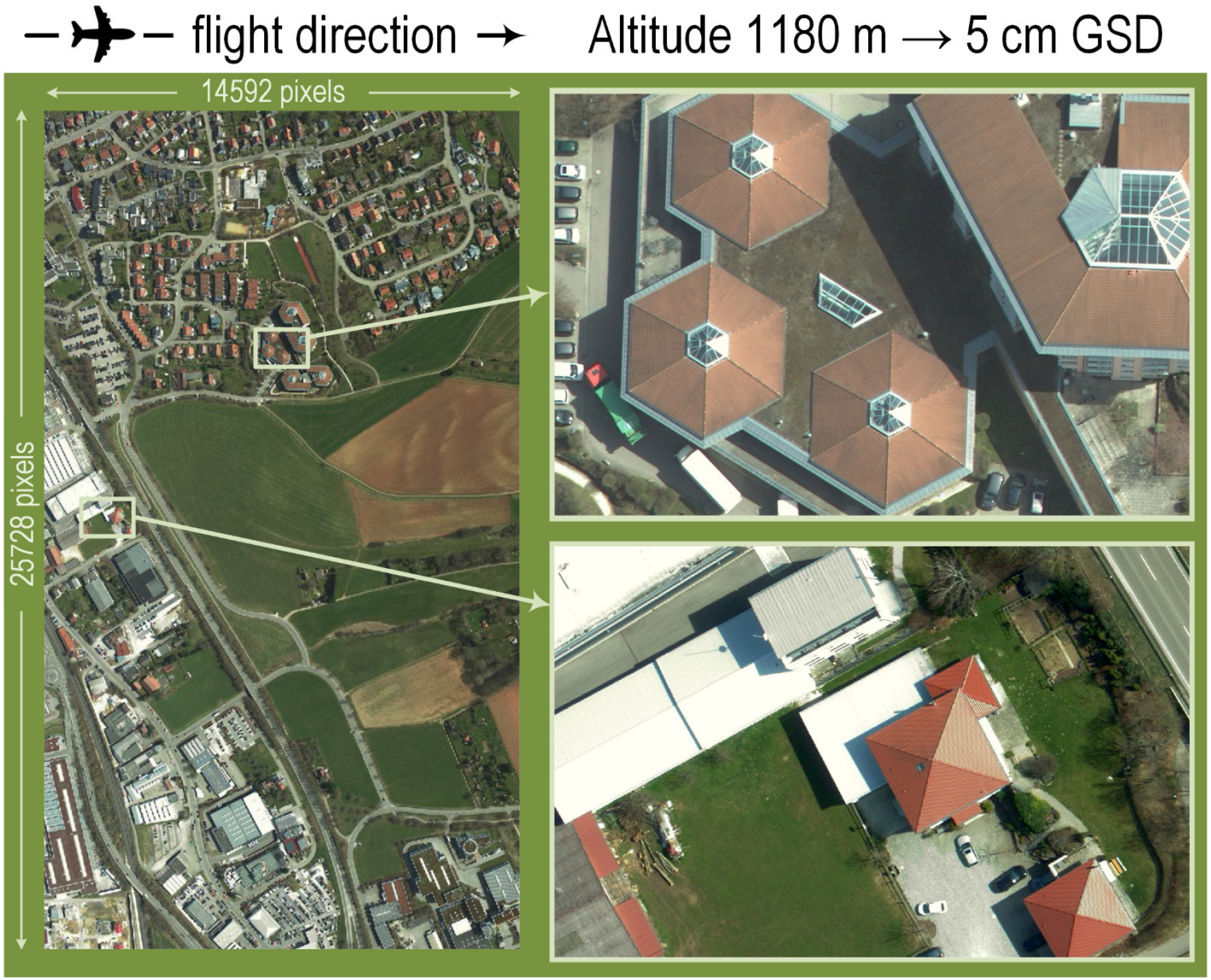
Example test flight 1



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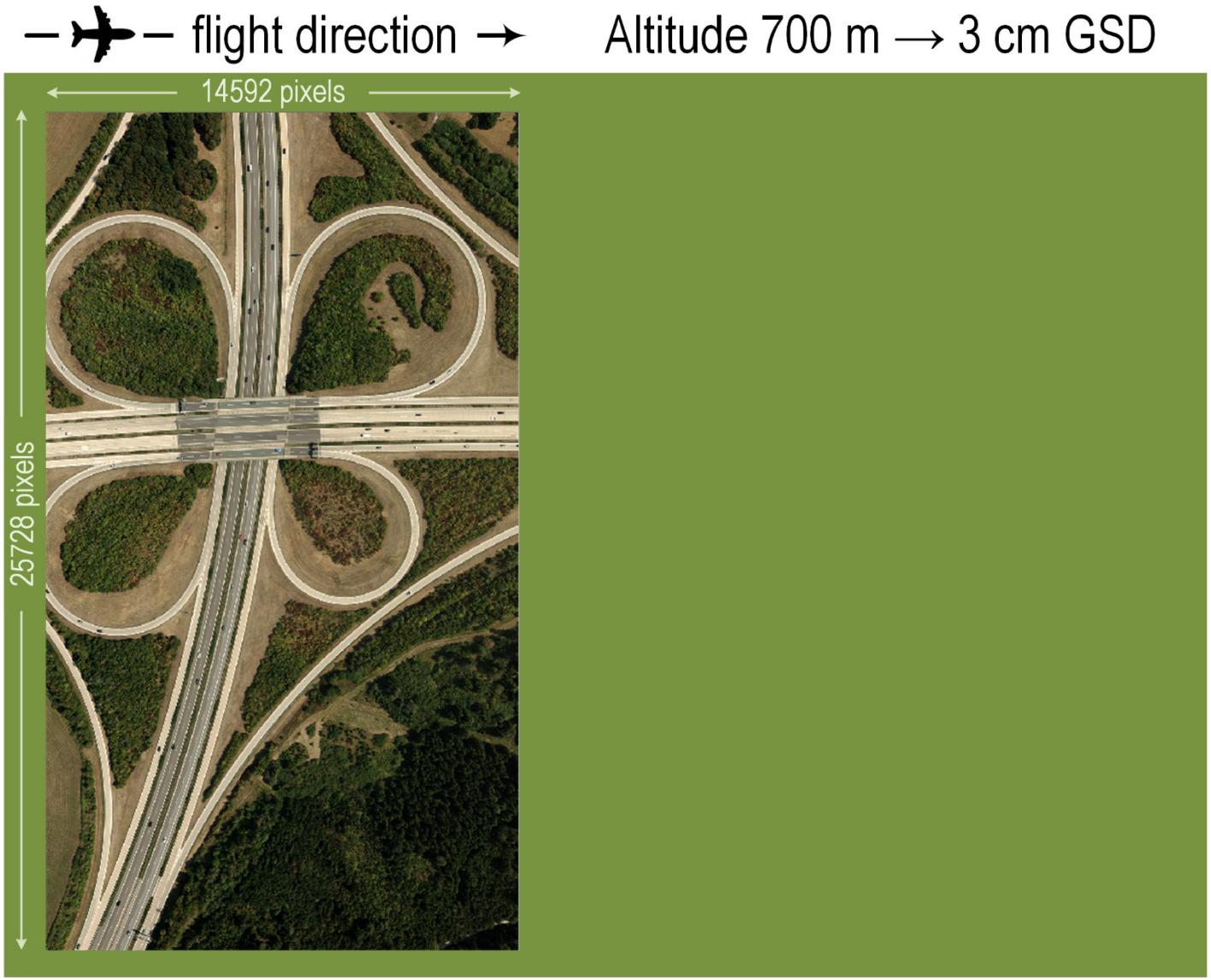
Example test flight 2



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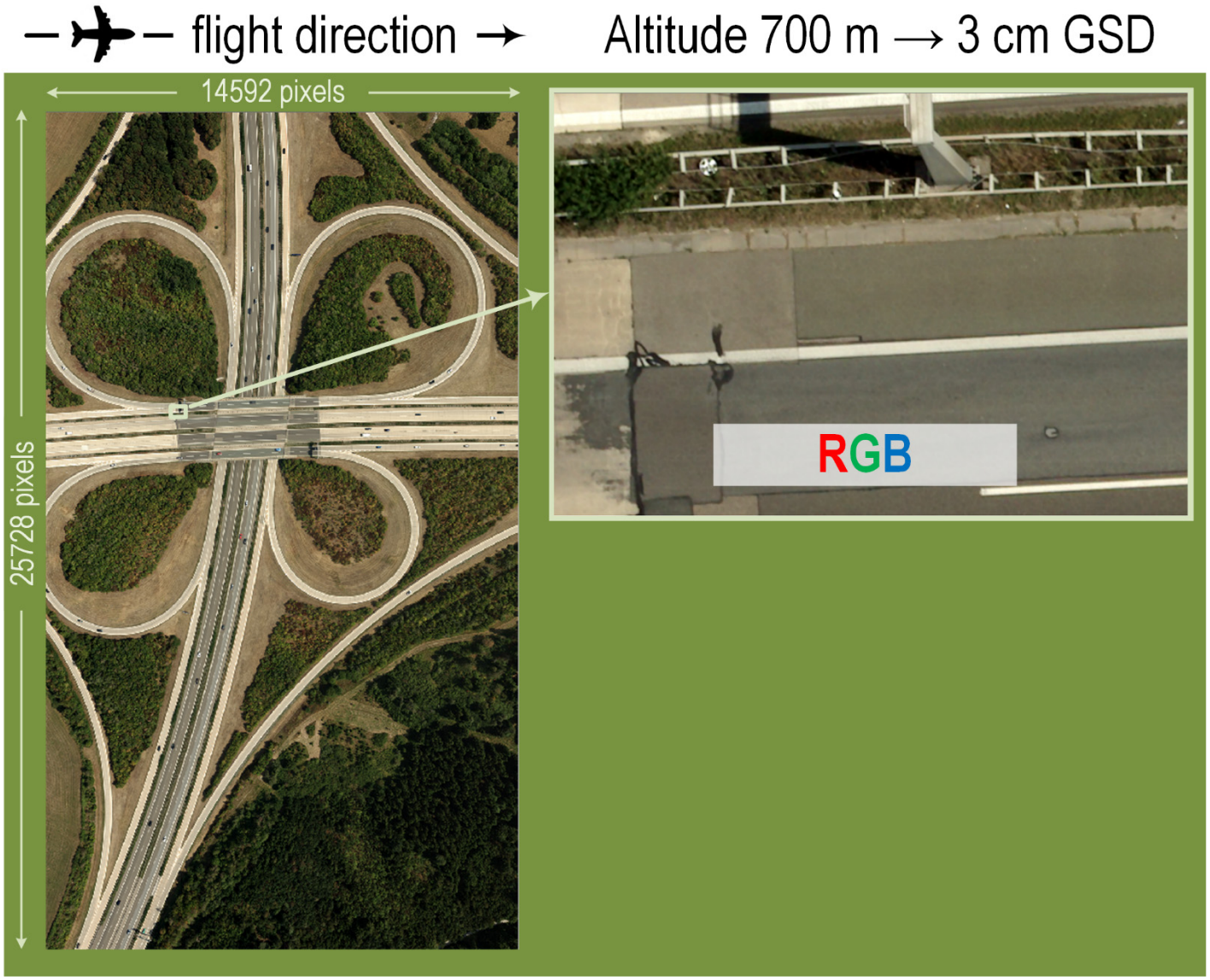
Example test flight 2



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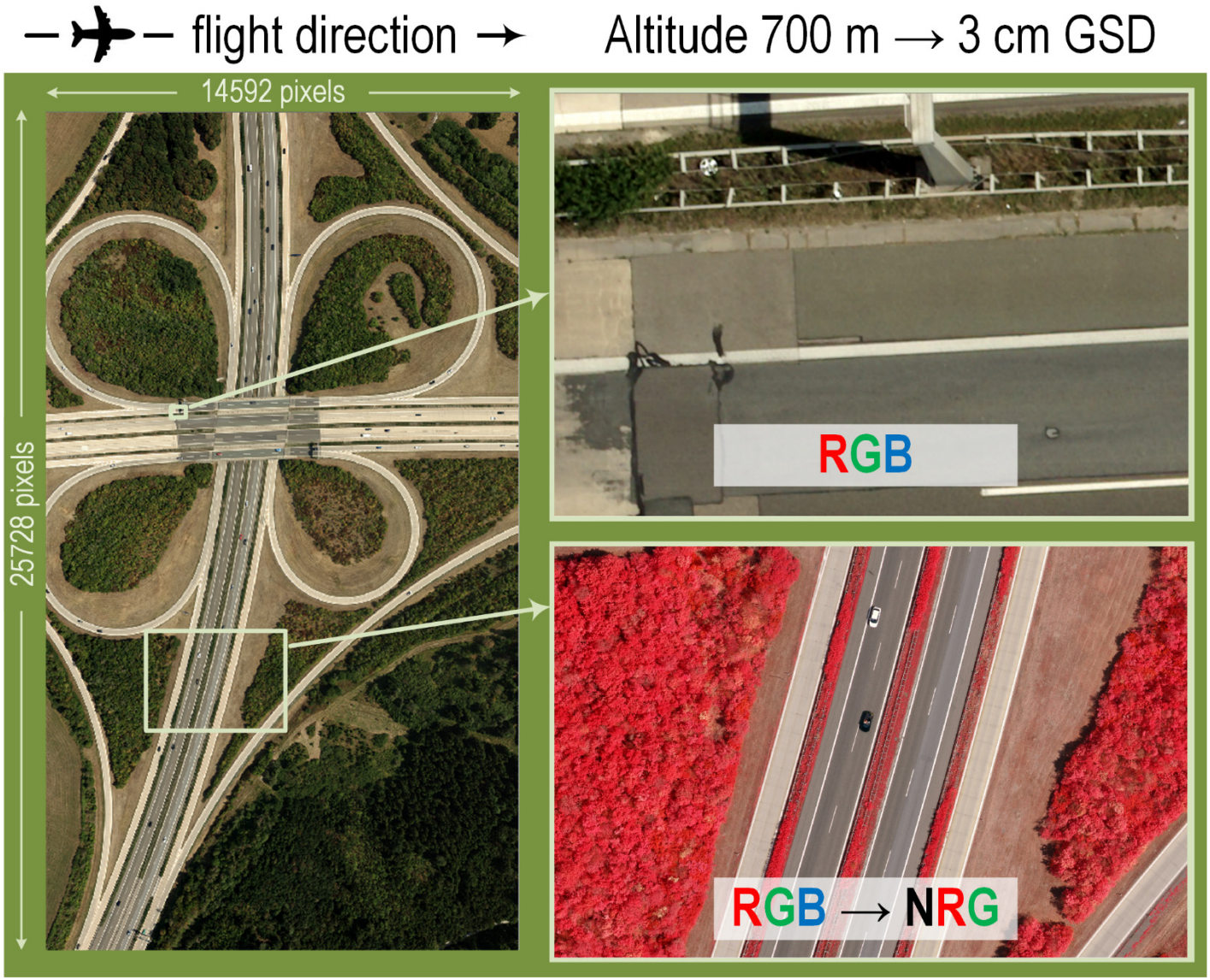
Example test flight 2



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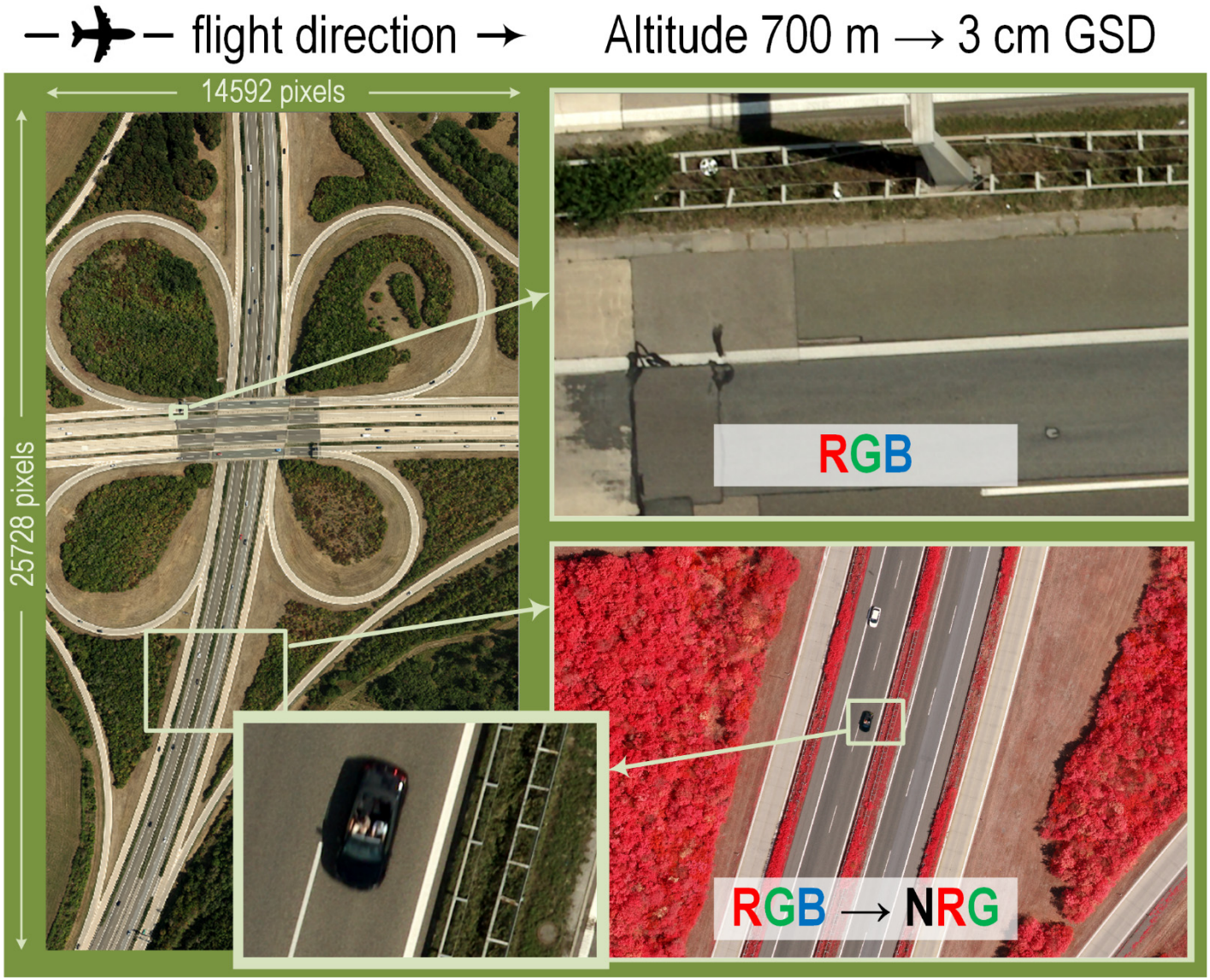
Example test flight 2



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Conclusions

- Large size, high resolution sensor using 2D stitching technology
- Highest pixel resolution sensor for aerial mapping: > 391 Mpixels
- Outperforms existing solutions:
  - Pitch: 3.9 µm
  - Linear FWC: 31.5 Ke-
  - Dark read noise: 3.7 e-
  - Linear DR: > 78 dB
  - QE: 75 % peak

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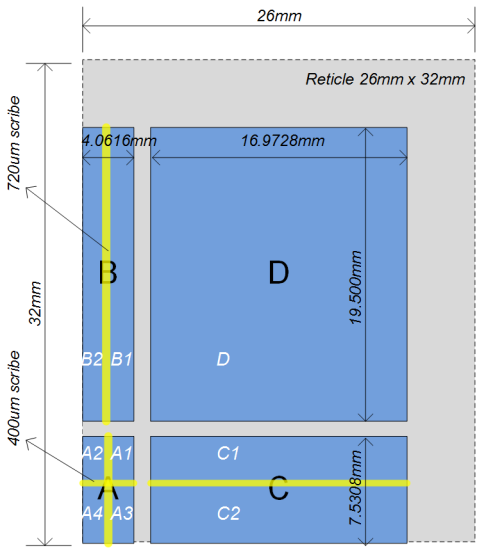
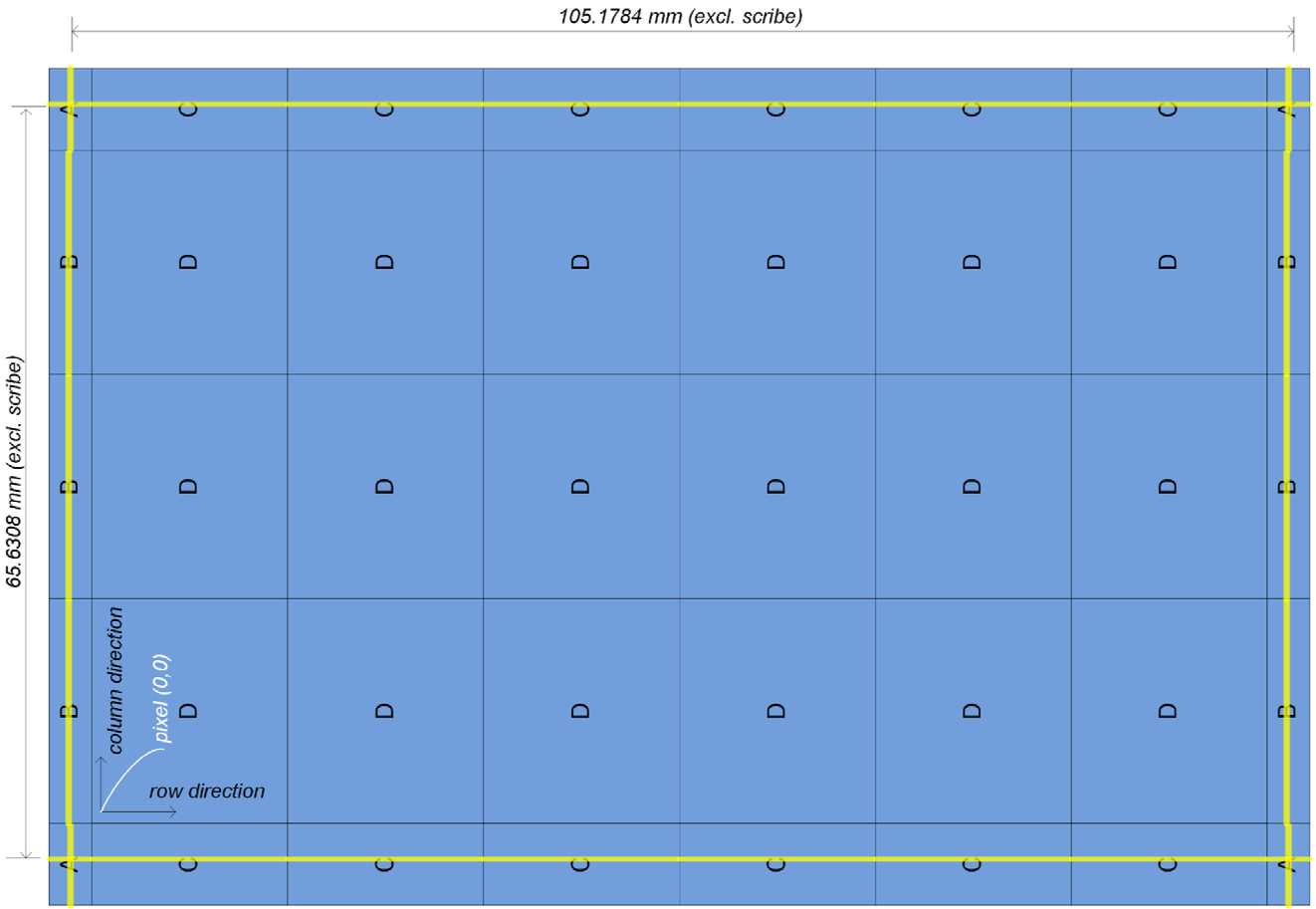
Q&A: 2D stitching technology

Reticle layout



Final sensor on wafer



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An APS-H-Size 250Mpixel CMOS Image Sensor Using Column Single-Slope ADCs with Dual-Gain Amplifiers

Hirofumi Totsuka, Toshiki Tsuboi, Takashi Muto,
Daisuke Yoshida, Yasushi Matsuno, Masanobu Ohmura,
Hidekazu Takahashi, Katsuhito Sakurai, Takeshi Ichikawa,
Hiroshi Yuzurihara, and Shunsuke Inoue

Canon Inc.

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Outline

- Background
  - Issues and Goal
- Technology
  - Block Diagram
  - Architecture of Column ADCs
  - Circuit & Timing
  - Compensation Process
- Results
  - Linearity Errors
  - Specifications
  - Image
- Summary

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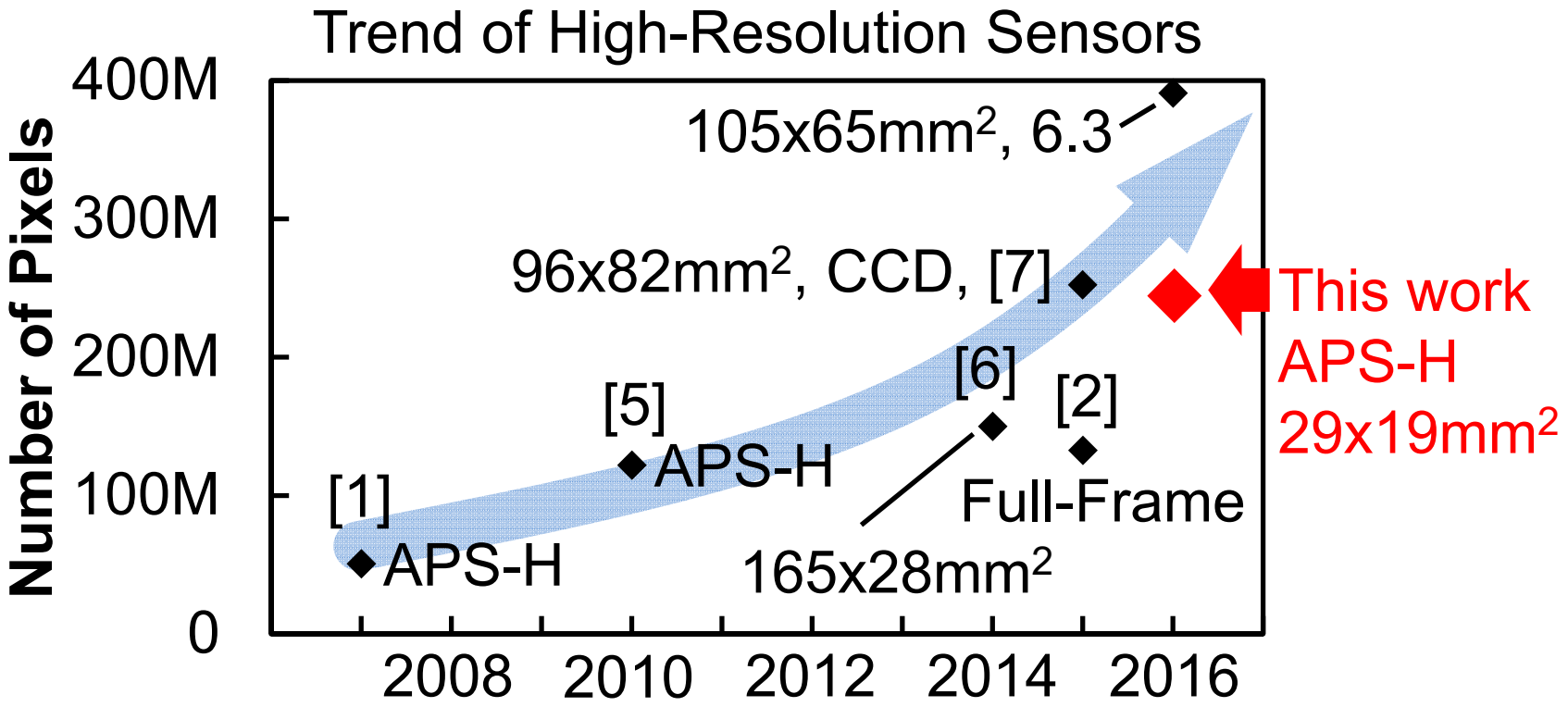
Background

- Demand for high-resolution sensors in various fields:
  - Specialized surveillance
  - Measuring instruments
  - Other industrial applications, etc.



[1] M. Iwane, IISW 2007
[2] R. Funatsu, ISSCC2015
[5] News Release, Canon Global in http://www.canon.com/news/2010/aug24e.html
[6] GMAX3005-GMAX series-Gpixel Inc. in http://www.gpixelinc.com/en/index.php?s=/b/42.html
[7] J. Bosiers, IISW2015.

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Issues of High-Resolution Sensors

- Speed of signal readout, limited by the following
  - Vertical readout
    (pixels → column circuits)
  - **AD conversion**
  - Horizontal readout
    (memories → internal signal processor)
  - Data output from the sensor

To ensure sufficient vertical readout period, speed-up of the AD conversion is essential.

- **Power consumption**
  - Proportional to the number of columns

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Scope and Goals

Scope

- Slope type ADC
  - Most popular architecture in commercialized CIS
- Approaches to speed-up the slope type ADC
  - Increase count clock frequency [3] → power increase
  - Use multiple slope signals [4] → severe quality control of the signals
  - etc.

Goals

- Develop a high-resolution sensor
- Column ADC suitable for high-resolution sensors
  - Fast AD conversion speed
  - Low power consumption

[3] T. Toyama, ISSCC2011
[4] M.F. Snoeji, ISSCC2007

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Outline

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  - Image
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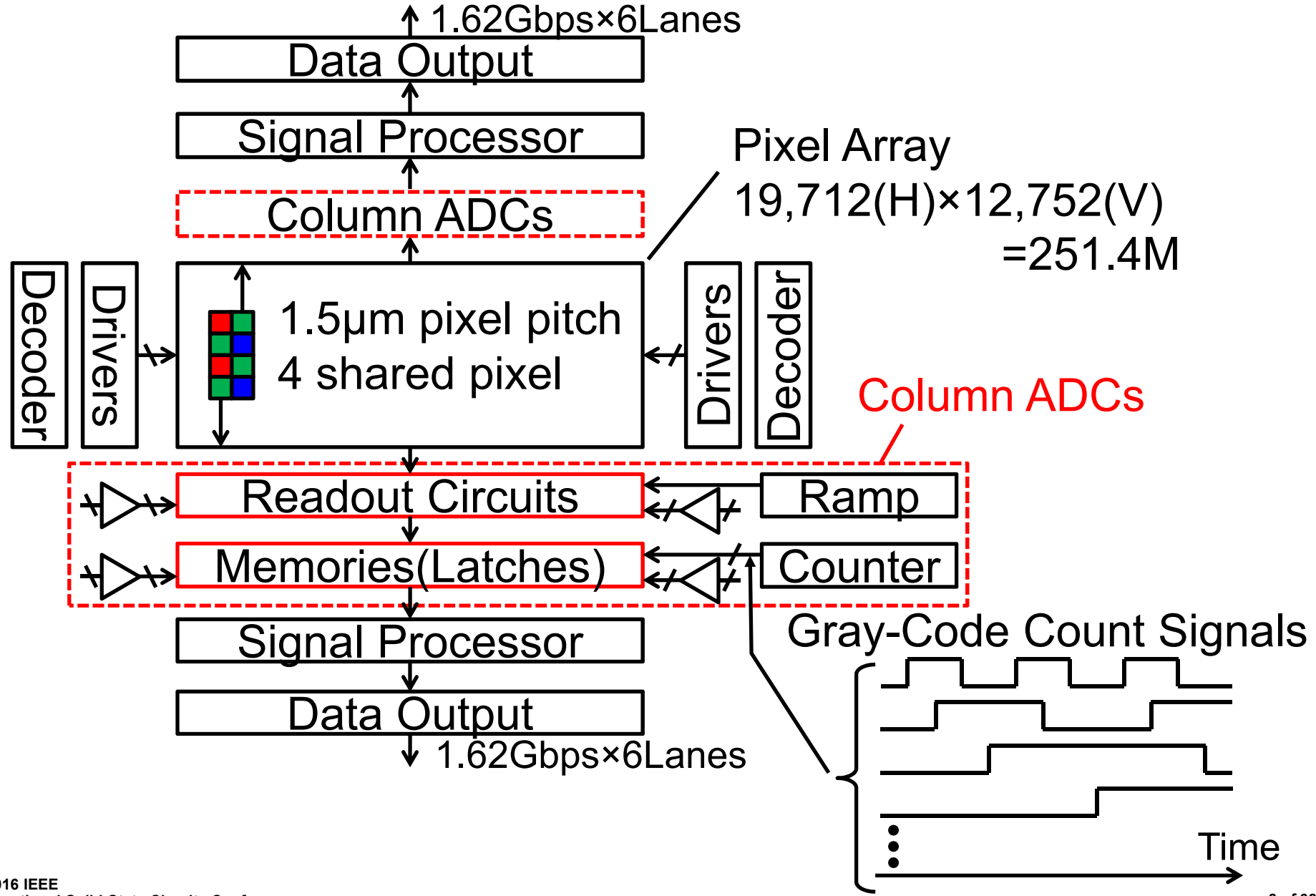
Block Diagram



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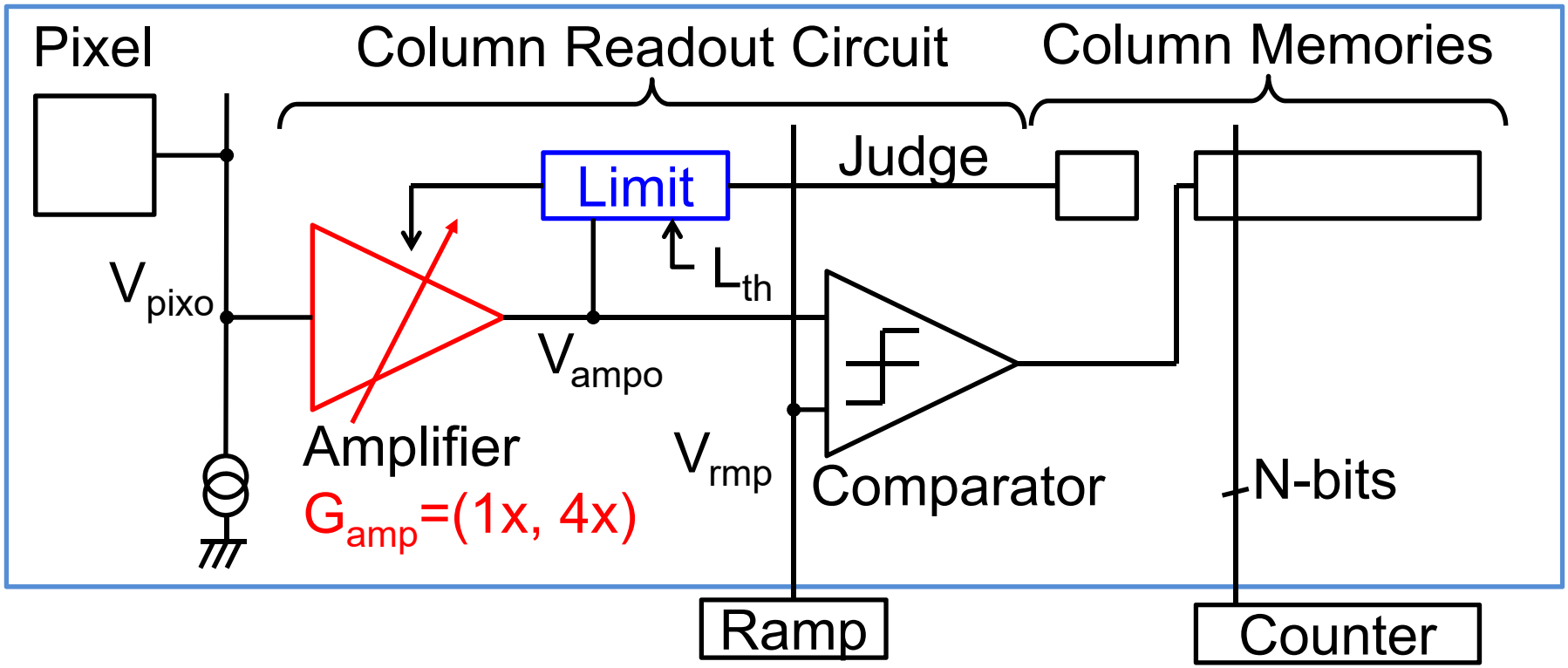
Single Slope ADC with Dual-Gain Amp

- Dual-gain amplifier (G_{amp}=1x, 4x)
- Limiting circuit
  - Compare V_{ampo} & the threshold (L_{th})
  - Control G_{amp}
- SSDG-ADC



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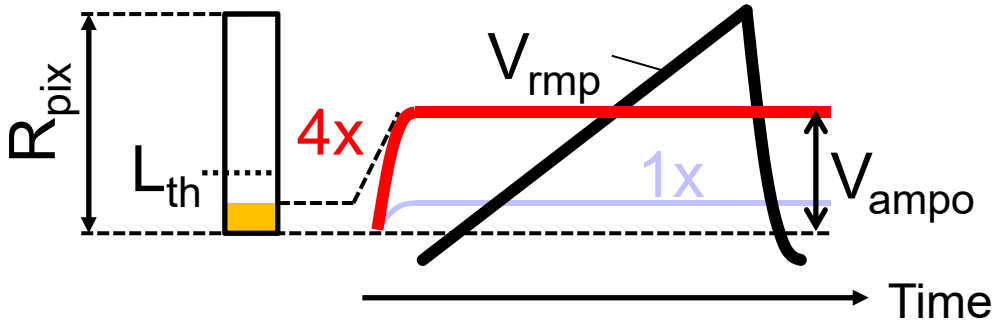
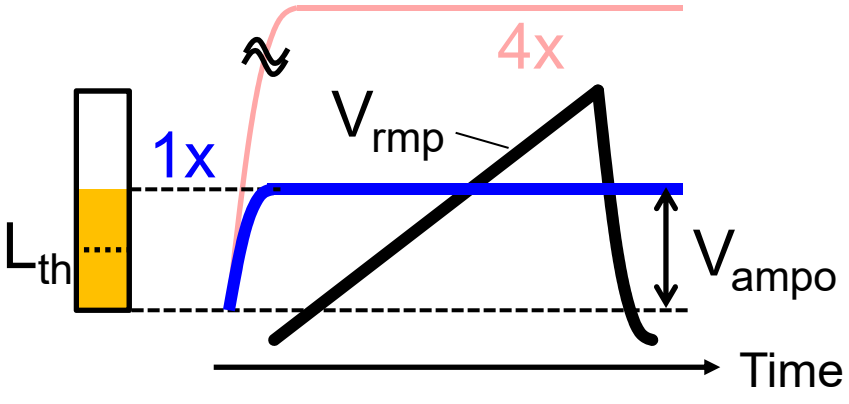
Concept of SSDG-ADC

12b-ADC

Low Light Level	High Light Level
	
Signal level < L_{th} (≈R_{pix}/4)	> L_{th} (≈R_{pix}/4)
G_{amp} 4x	1x
Digital gain 1x	4x

R_{pix}; Signal range of the pixel
L_{th}=~1/4×R_{pix}, ~1,000 [LSB]

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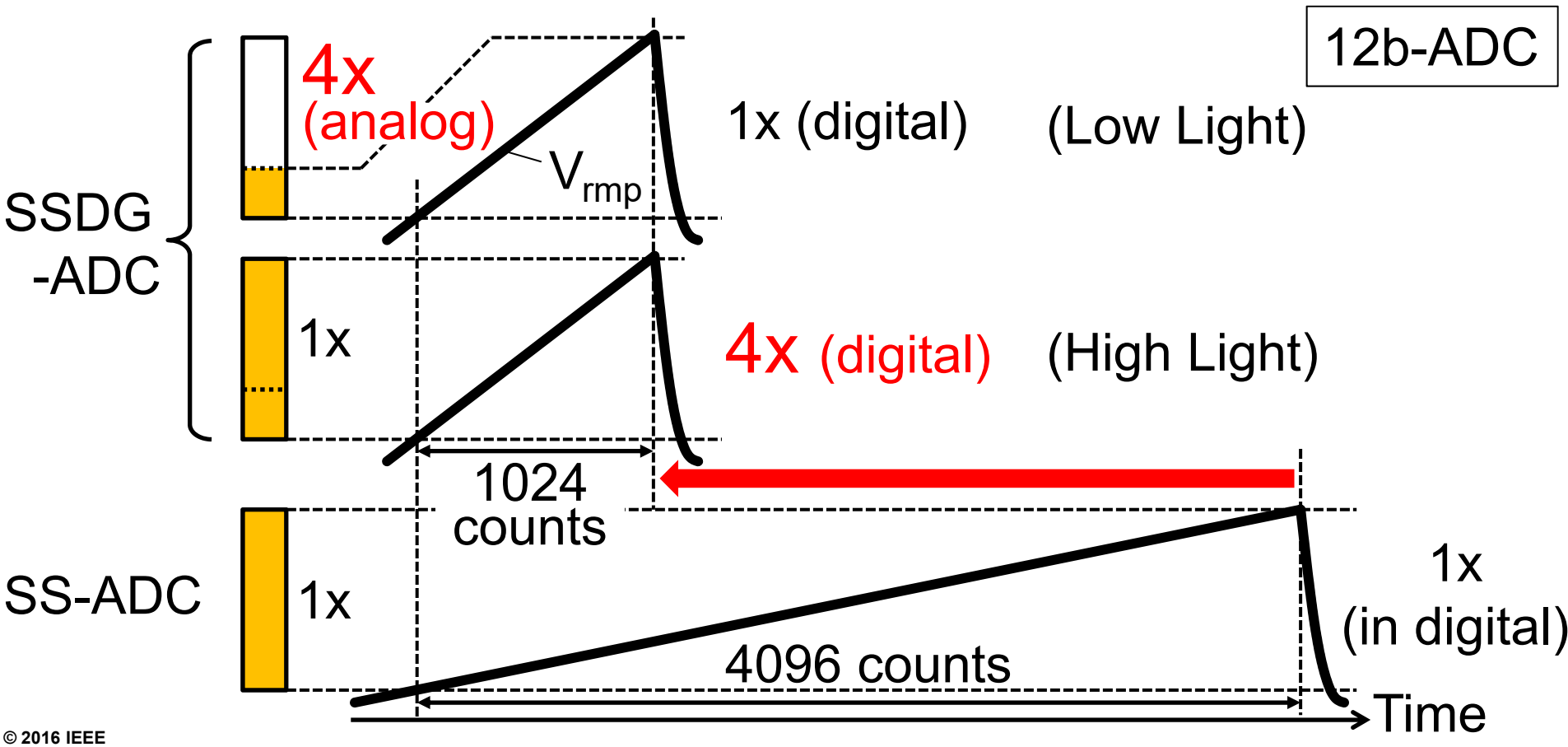
SSDG-ADC vs. SS-ADC

- ~4x faster AD conversion speed
- Wider dynamic range

$$\text{Dynamic Range} = \frac{\text{(input referred) Dark RN}}{\text{Signal Range @ Pixel}}$$



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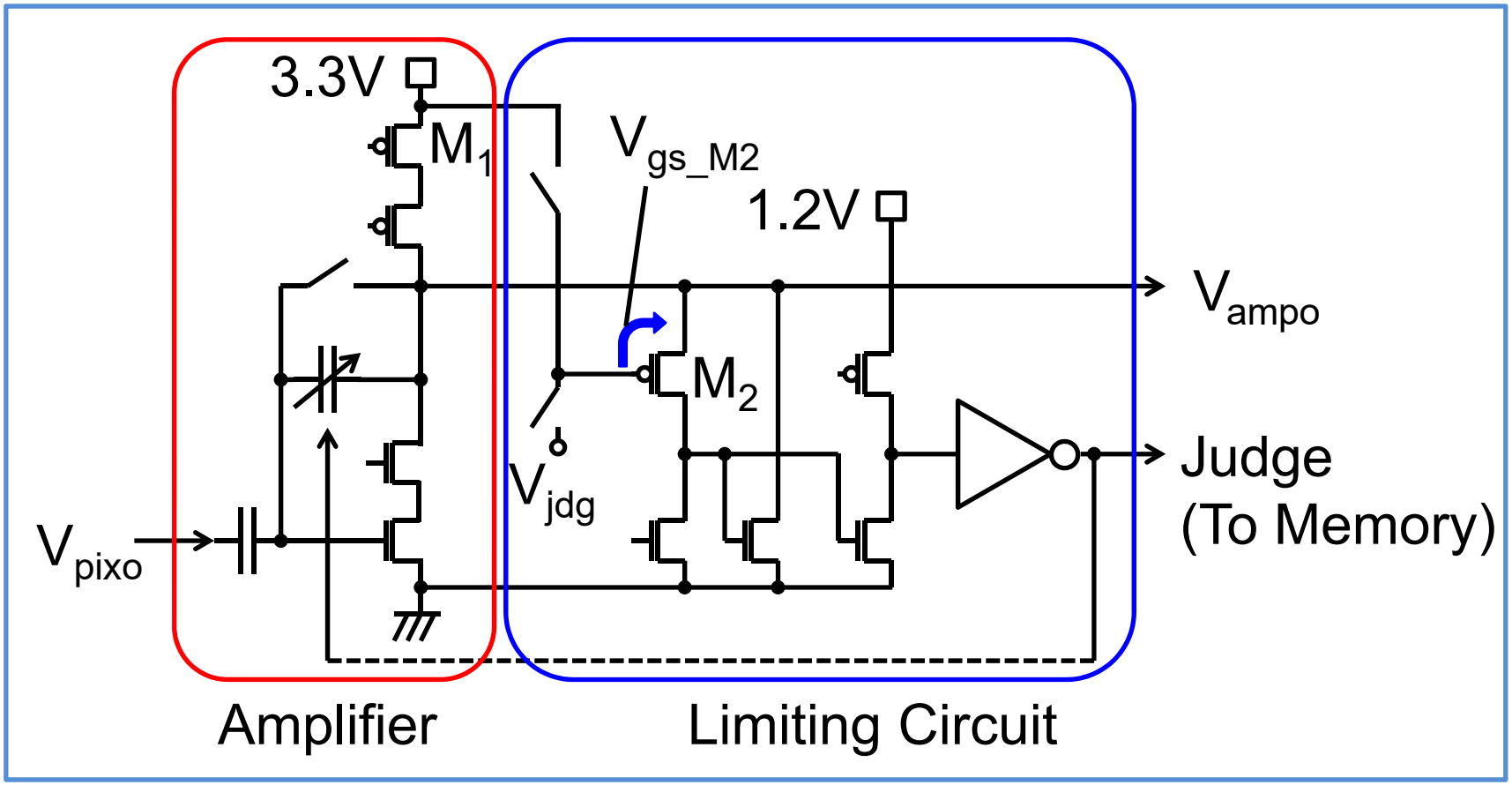
Amplifier & Limiting Circuit

- The threshold $L_{th} = V_{jdg} + V_{gs\_M2}$
- Clipping V_{ampo} for avoiding the amp's saturation
- Negligible power increase due to the limiting circuit



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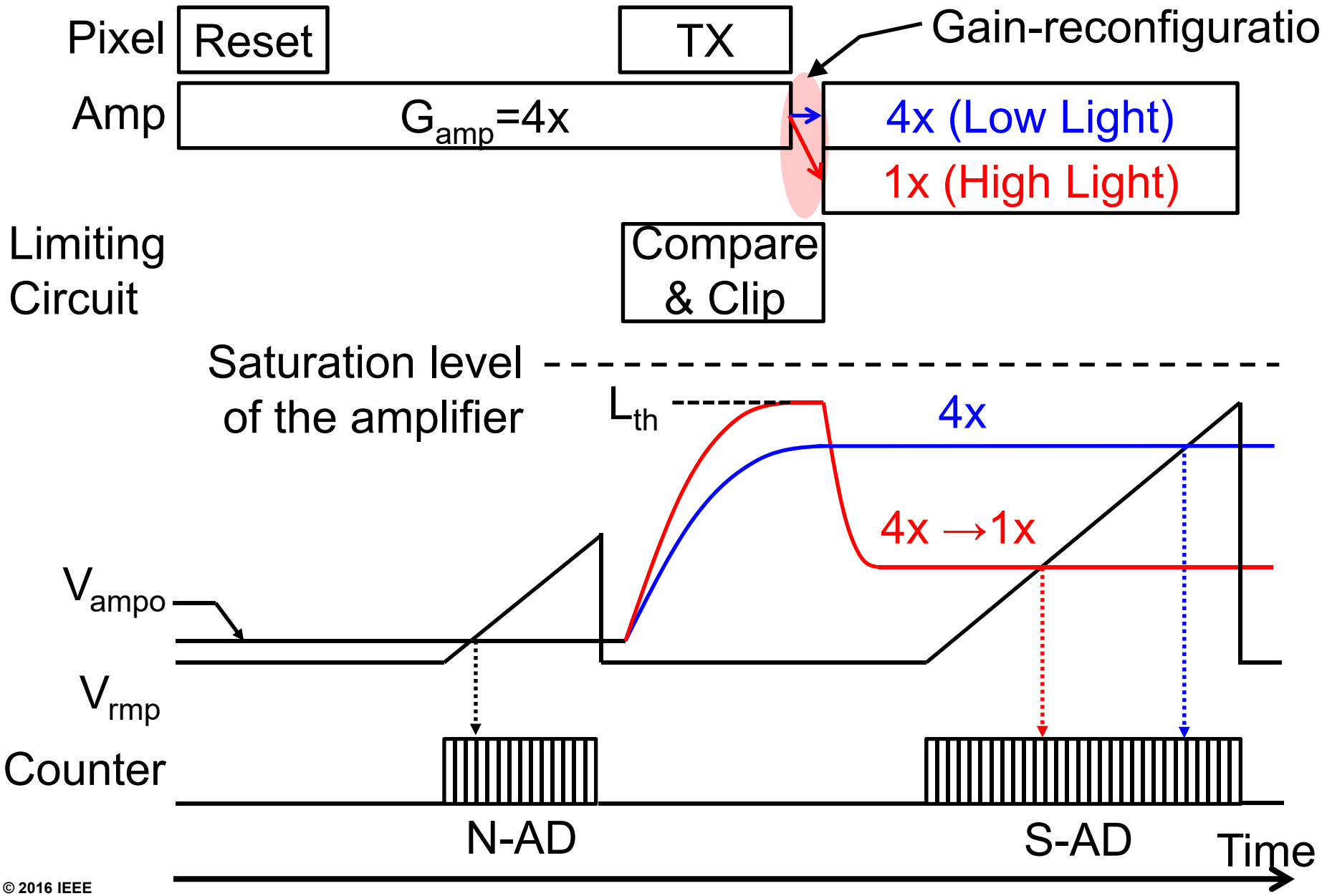
Timing Diagram



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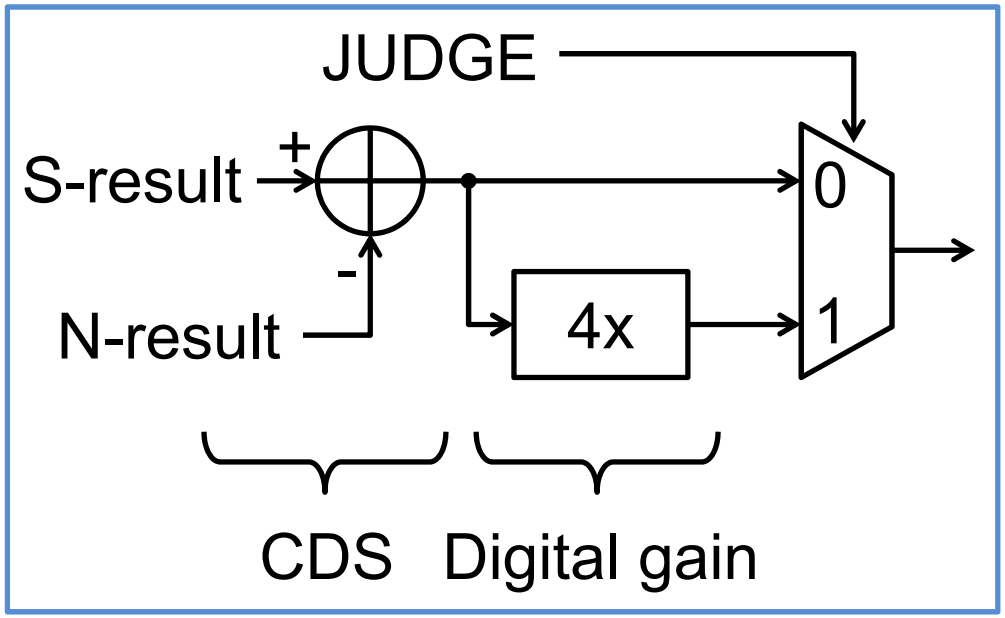
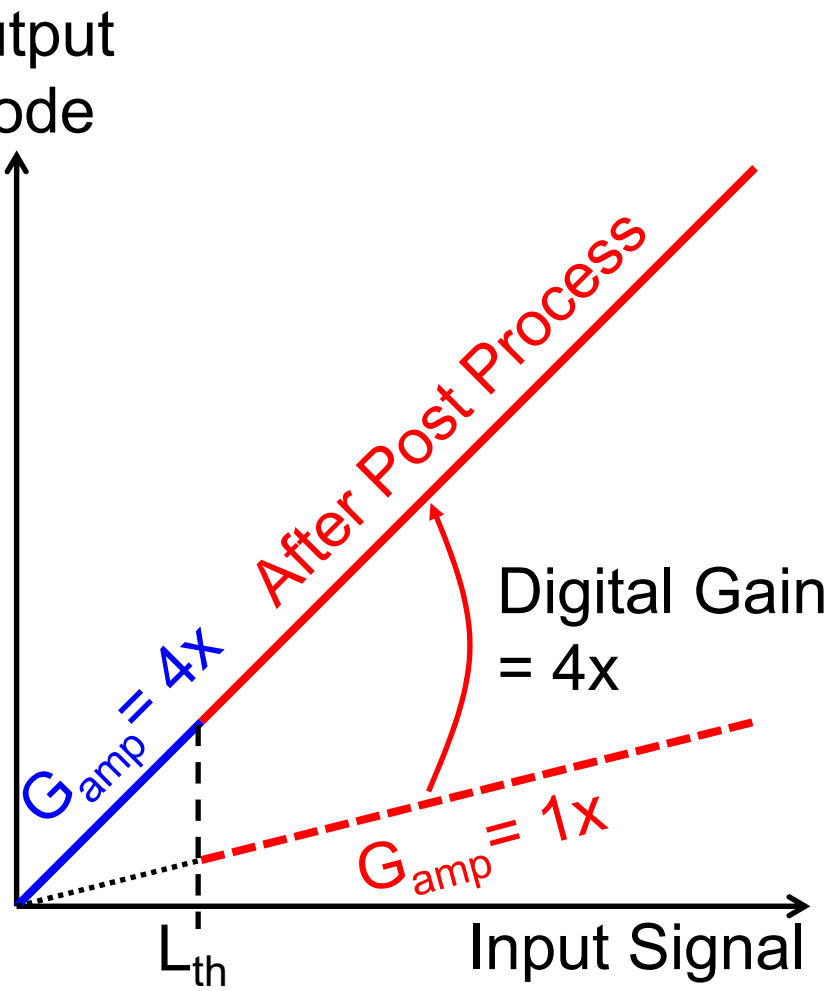
Post Signal Process

- Correlated Double Sampling (CDS); (S-AD) - (N-AD)
- High-light result is multiplied by 4

@ Signal Processor





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Linearity Errors

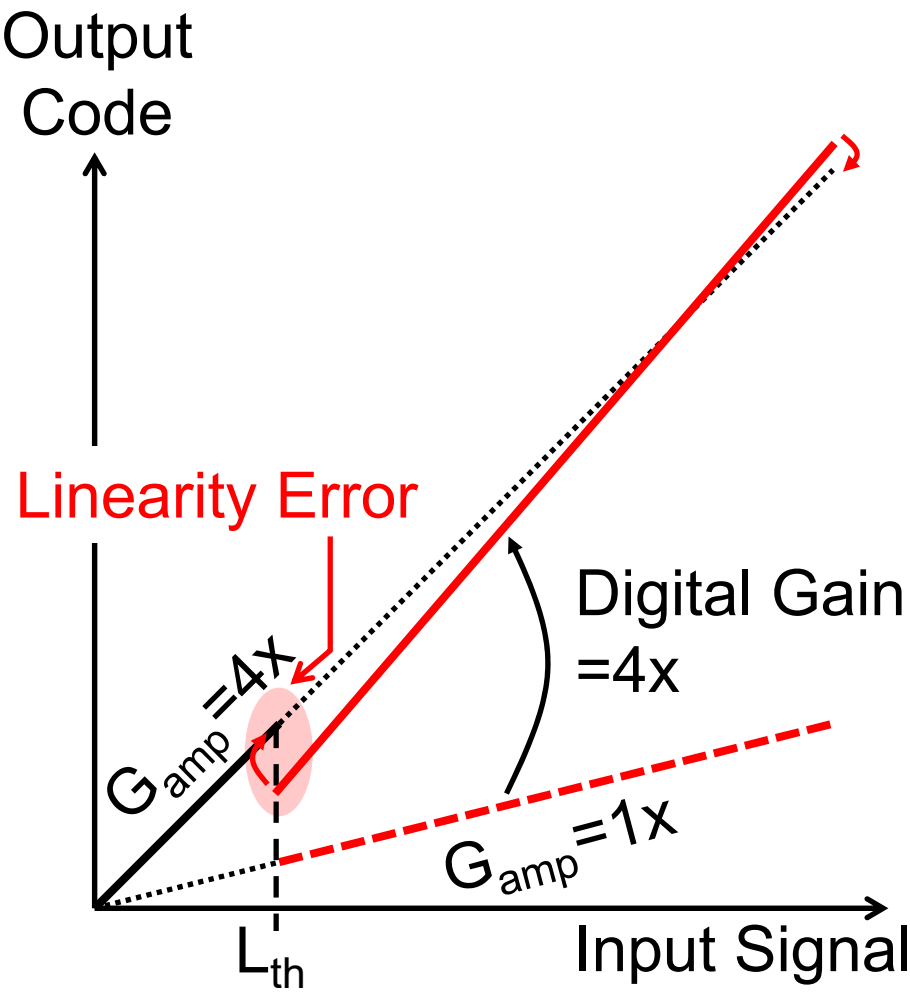
Linearity Errors (DNL at L_{th}) may occur.

- Gain and offset deviations at the amplifiers

If the errors are visible,

Compensation process

- Data acquisition
- Coefficients calculation
- Compensation for the errors



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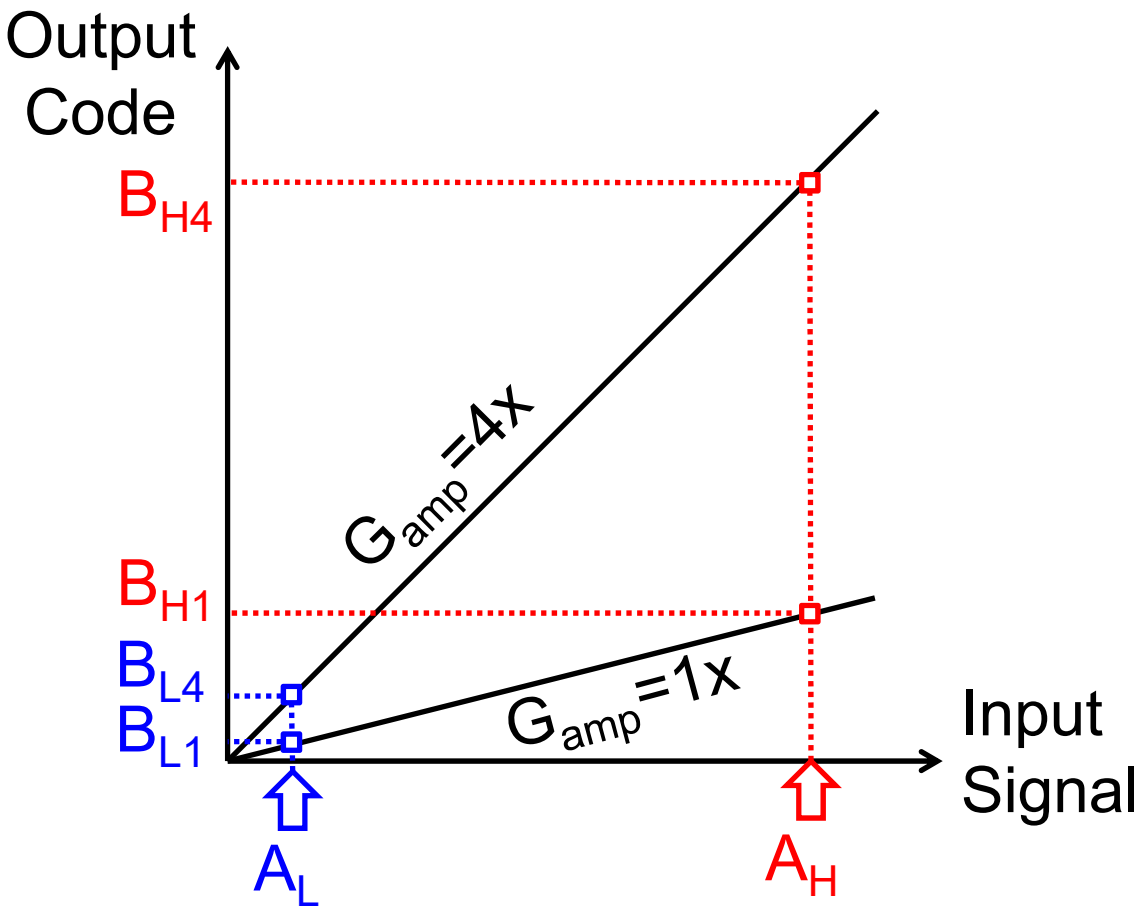
Compensation Process (1)

- Data acquisition
  - Measure two known levels (A_L & A_H) with two G_{amp}(1x & 4x)
  - Get 4 results (B_{L1},B_{H1},B_{L4} & B_{H4}) in each column



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Compensation process (2)

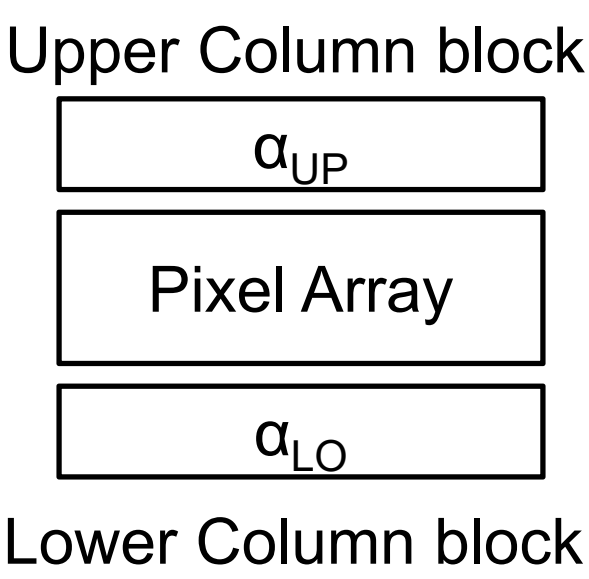
Coefficients calculation

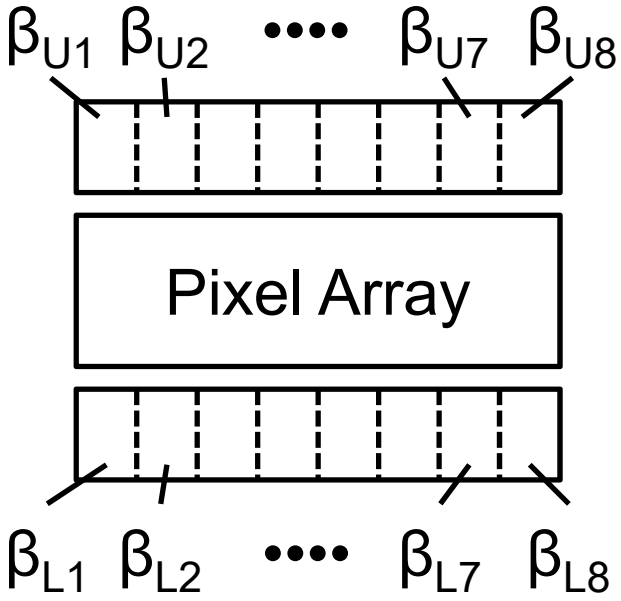
- Gain coefficient α

$$\alpha = \frac{B_{H4} - B_{L4}}{4 \times (B_{H1} - B_{L1})}$$

- Offset coefficient β

$$\beta = B_{L4} - 4 \times B_{L1} \times \alpha$$





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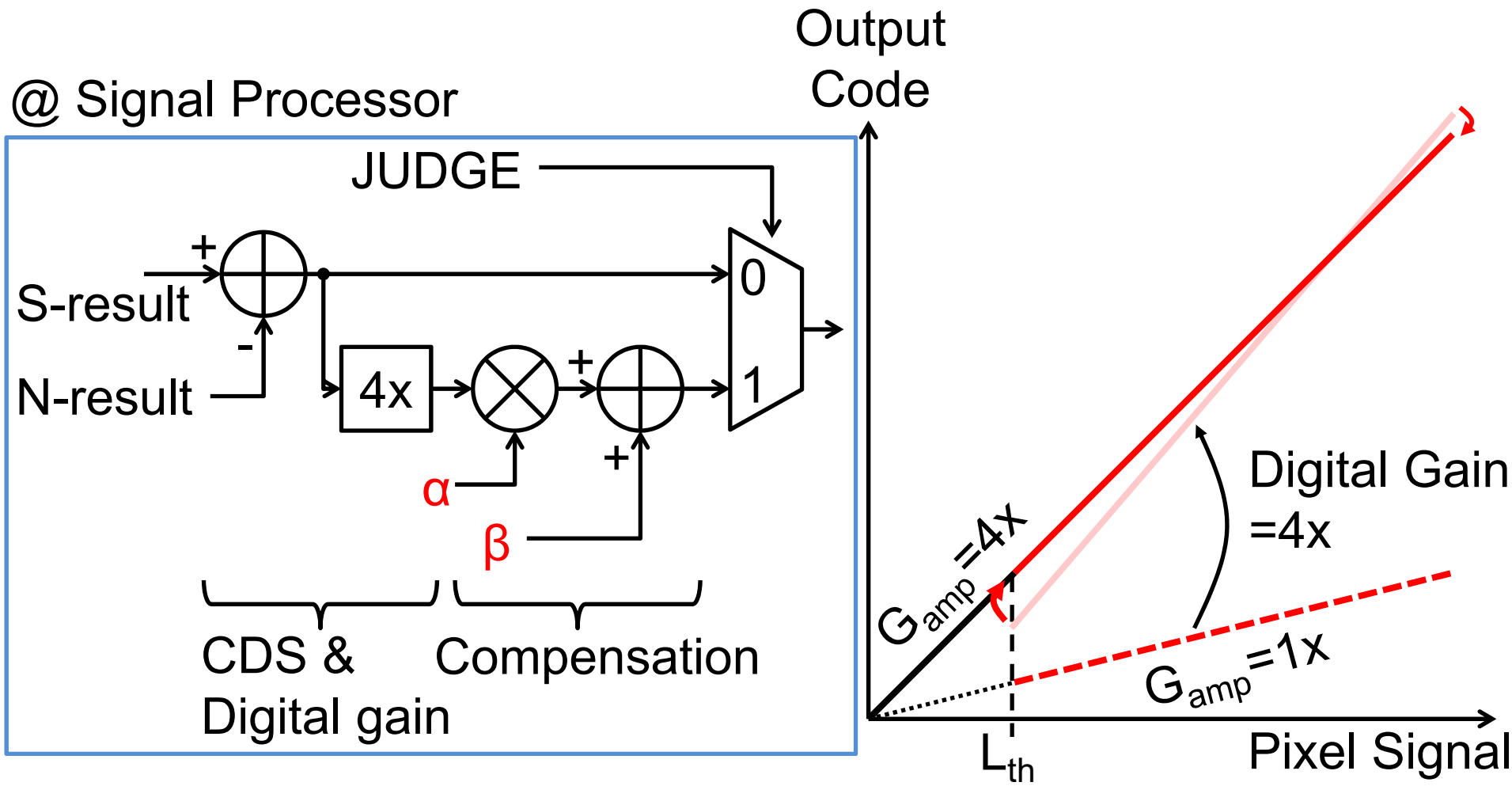
Compensation Process (3)

- Compensate high-light results for the linearity errors by 4×(S_AD-N_AD)×α+β



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Outline

- Background
  - Issues and Goal
- Technology
  - Block Diagram
  - Architecture of Column ADCs
  - Circuit & Timing
  - Compensation Process
- **Results**
  - **Linearity Errors**
  - **Specifications**
  - **Image**
- Summary

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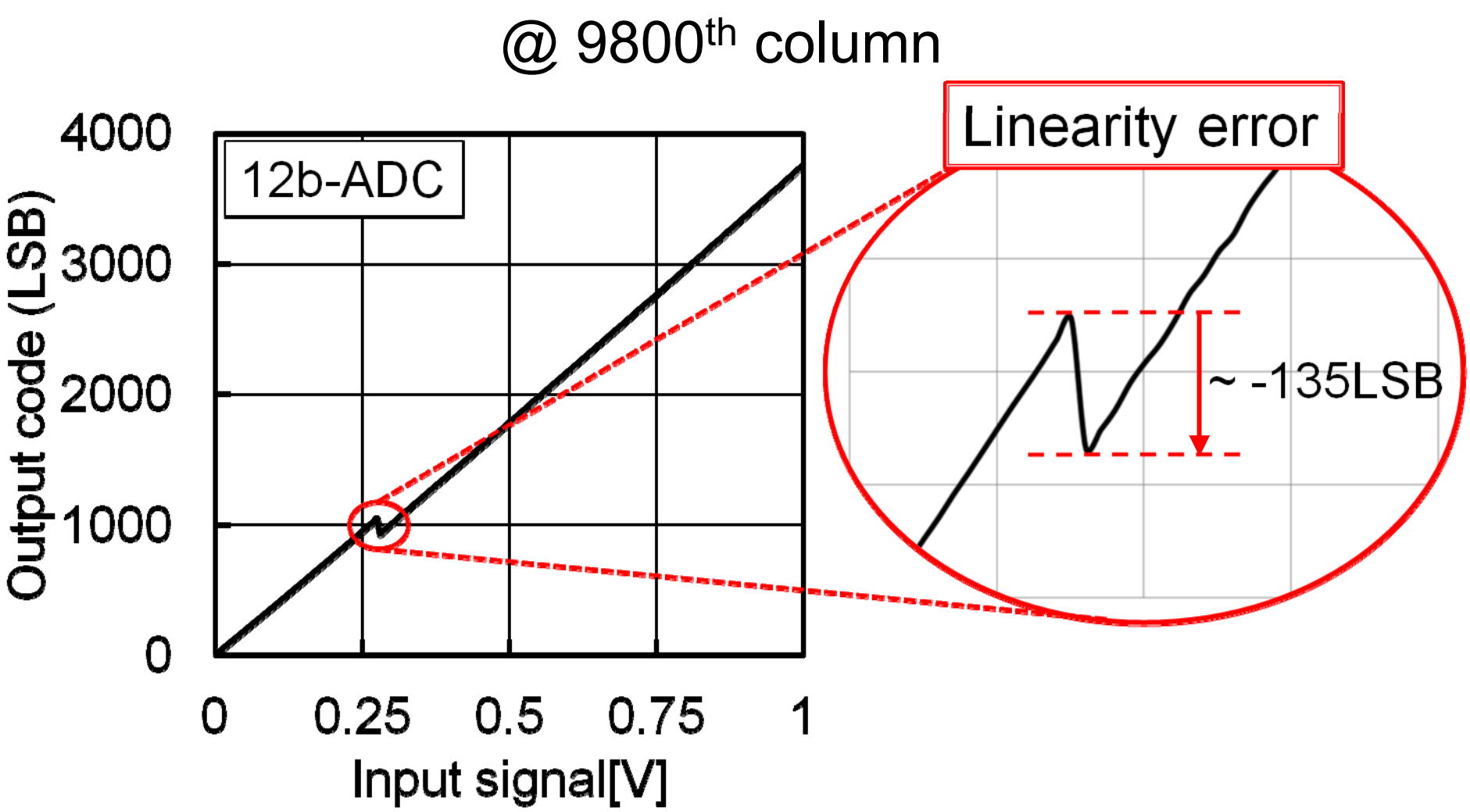
Input/Output Characteristics



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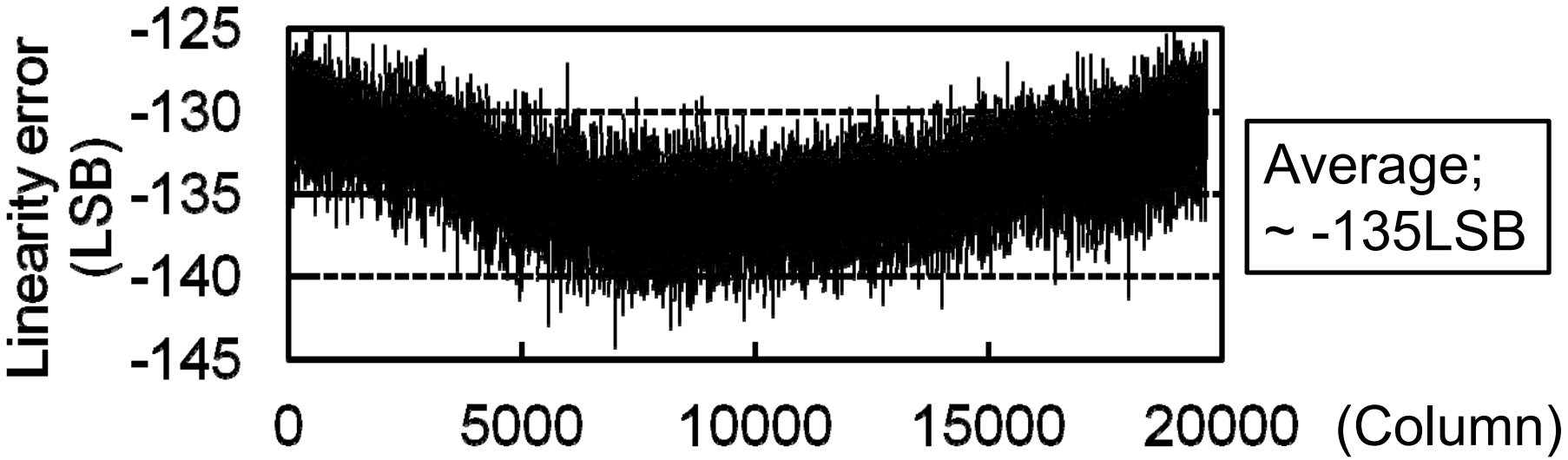
Measured Linearity Errors

- Without Compensation

12b-ADC



Average;
~ -135LSB

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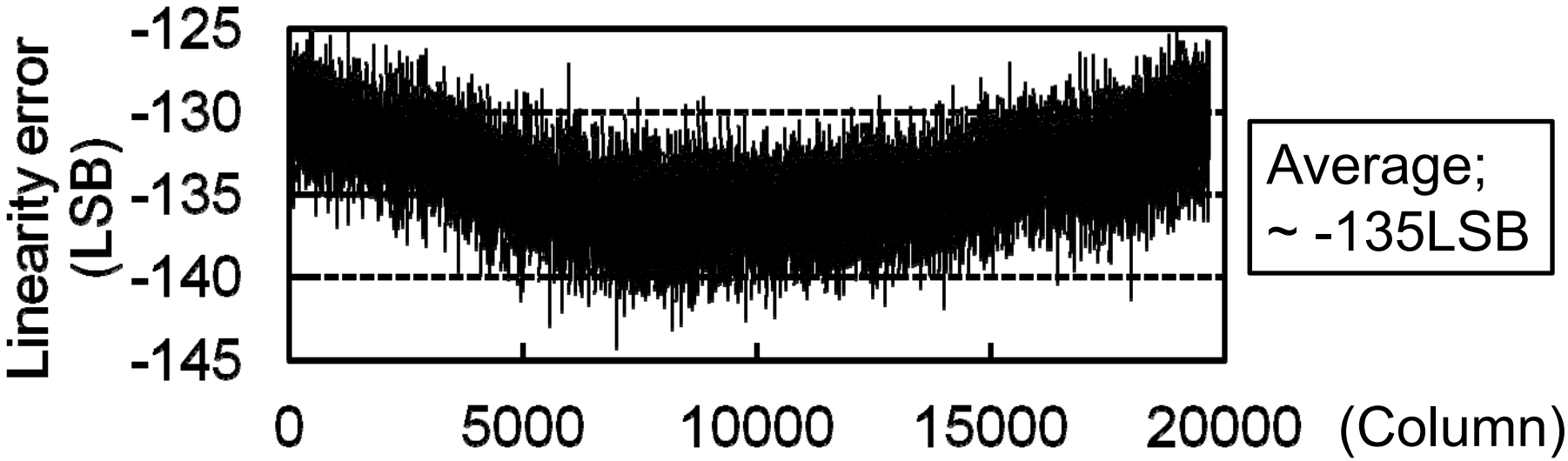
Measured Linearity Errors

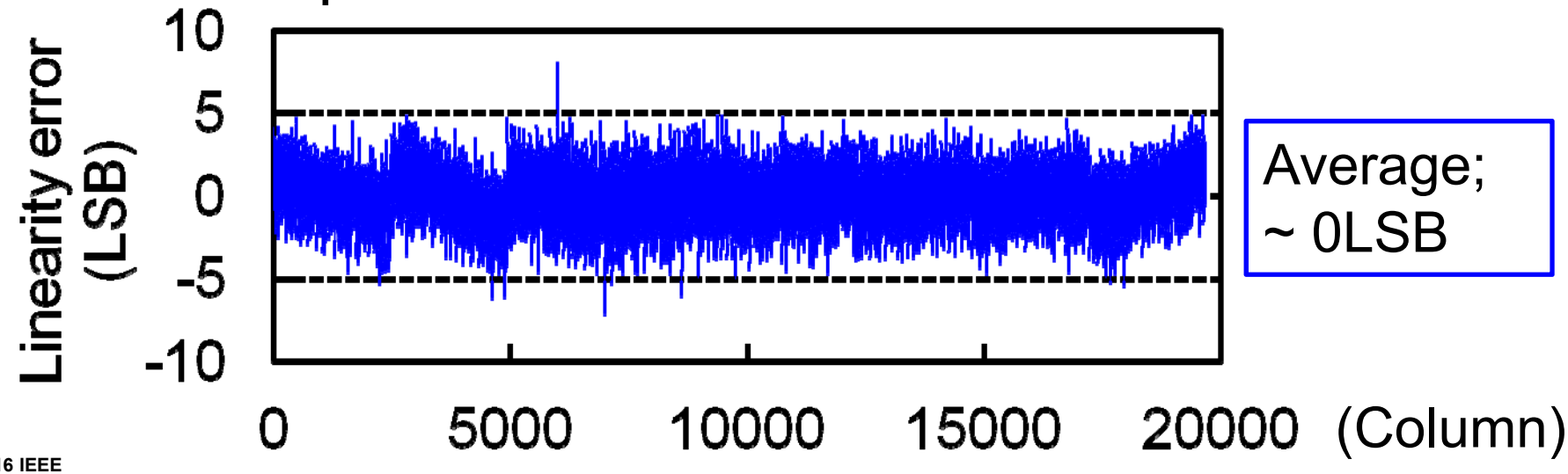
Without Compensation

12b-ADC



Average;
~ -135LSB

With Compensation



Average;
~ 0LSB

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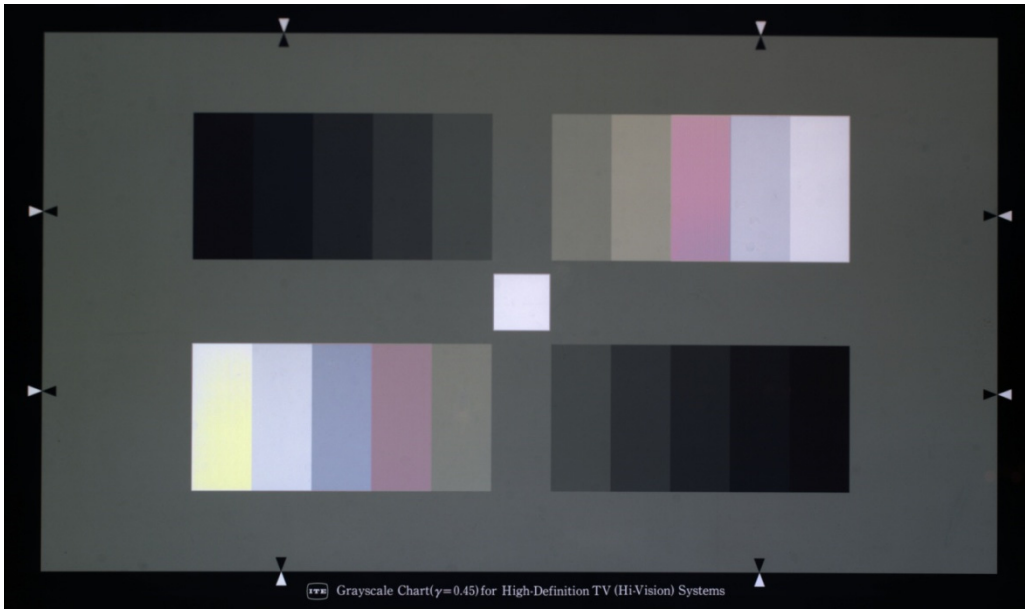
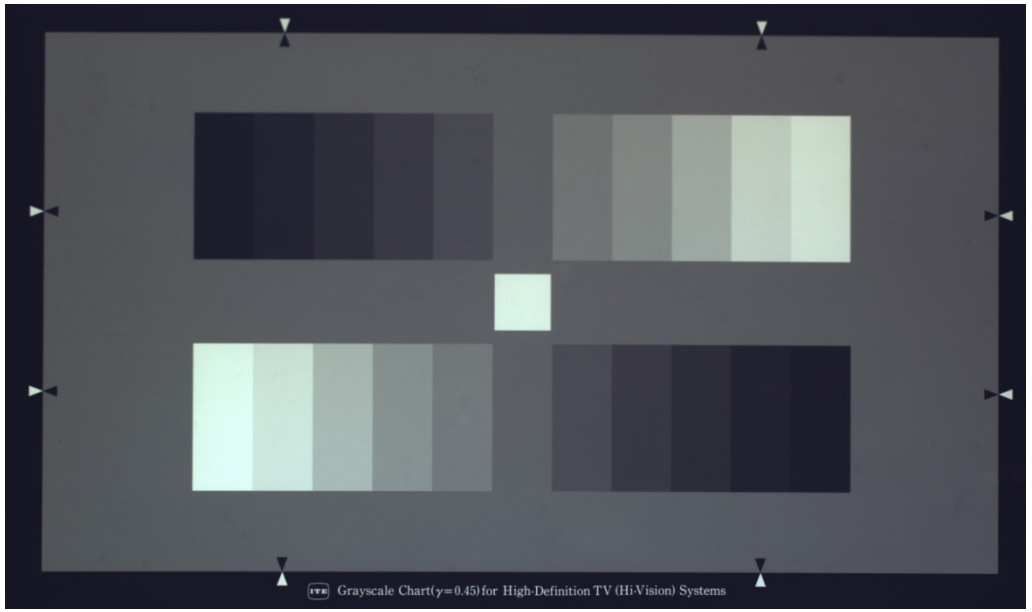
Compensation Effect

Without the compensation



With the compensation



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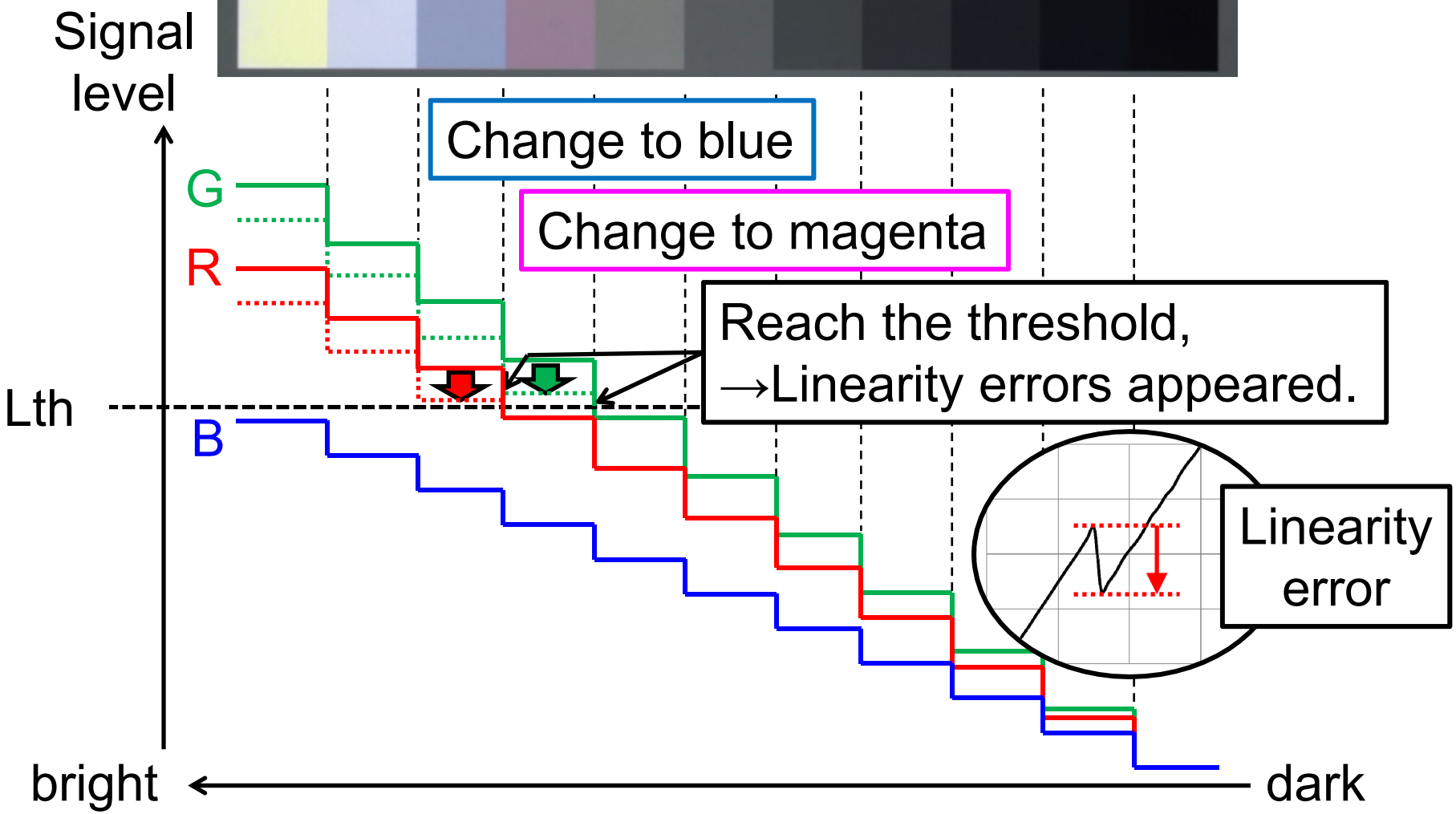
Why the colors changed?



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Effect of faster AD conversion speed

- Improvement in AD-resolution and frame rate

@ 250M pixel readout

- Frame rate = 5fps

	SS	SSDG
AD resolution	10-b	12-b

- AD resolution = 12-b

	SS	SSDG
Frame rate	3.8 fps	5.0 fps

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Specifications

Process		0.13 μm 1P4M CMOS
Power supply		3.3 V / 1.2 V
Die size		32.84 mm x 25.84 mm
Number of pixels	Total	19,712(H) x 12,752(V) =251.4M pixels
	Valid	19,568(H) x 12,588(V) =246.3M pixels
Pixel size		1.5 μm x 1.5 μm
Maximum frame rate	Full pixel	5 fps
	8K4K※	24 fps
	4K2K※	48 fps
Frequency of ADC count clock		810M Hz

※Cropped

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Characteristics

@ 250M pixel readout, 5fps

Conversion Mode	SS-ADC	SSDG-ADC
Power consumption @Full pixels	1.97 W (Pixel: ~40%, Comparator: ~30%, Amplifier: ~15%, Others: ~15%)	
Sensitivity	4,100 e^-/lx/sec	
Full Well Capacity	7,550 e^-	
Dark Current	7 e^-/sec @60 °C	
Conversion Gain	91 μV/e^-	
ADC resolution	10-b	12-b
Dark Random noise	7.1 e^-_{rms}	3.5 e^-_{rms}
Dynamic range	60.5 dB	66.7 dB

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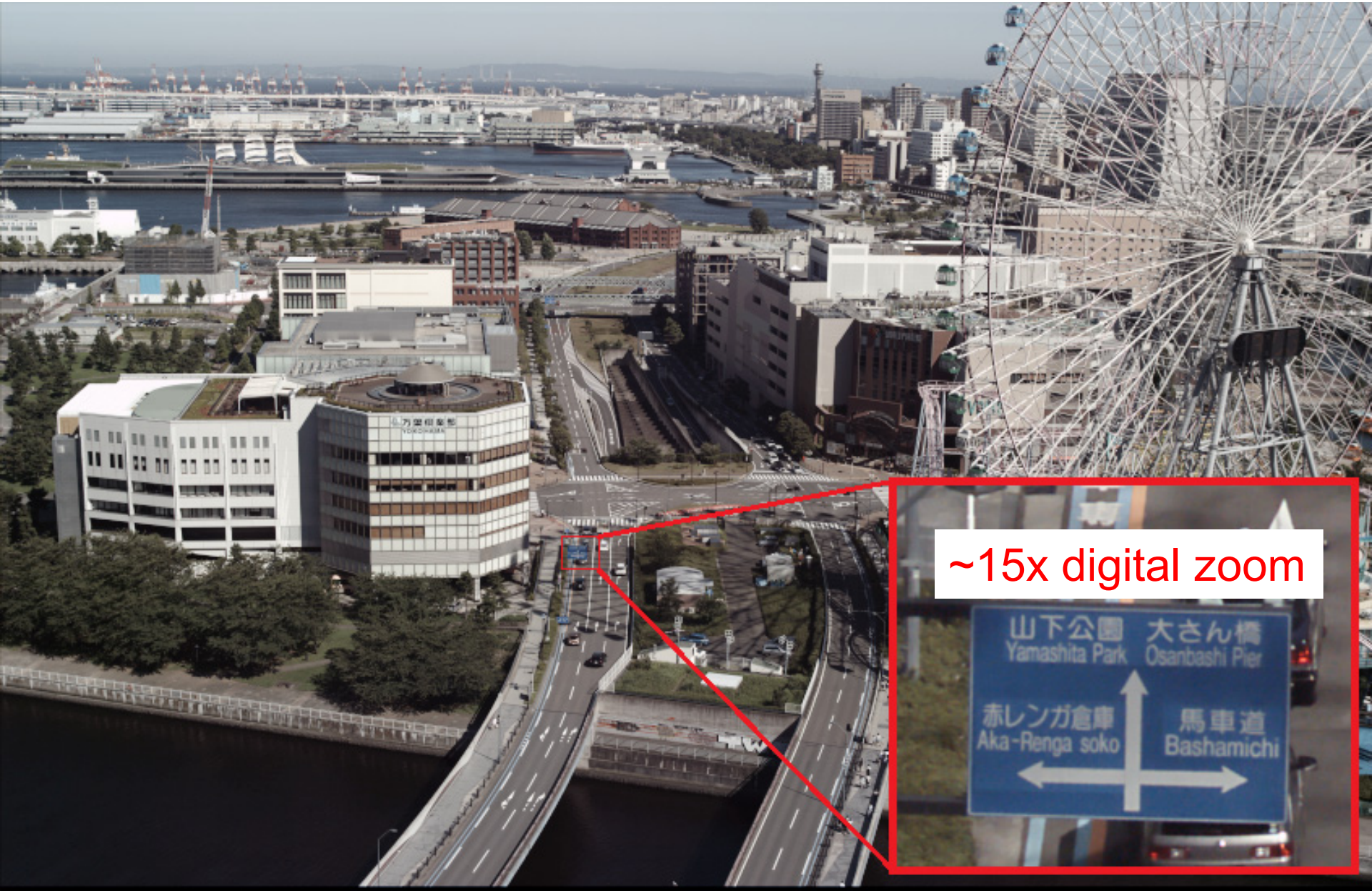
Reproduced Image



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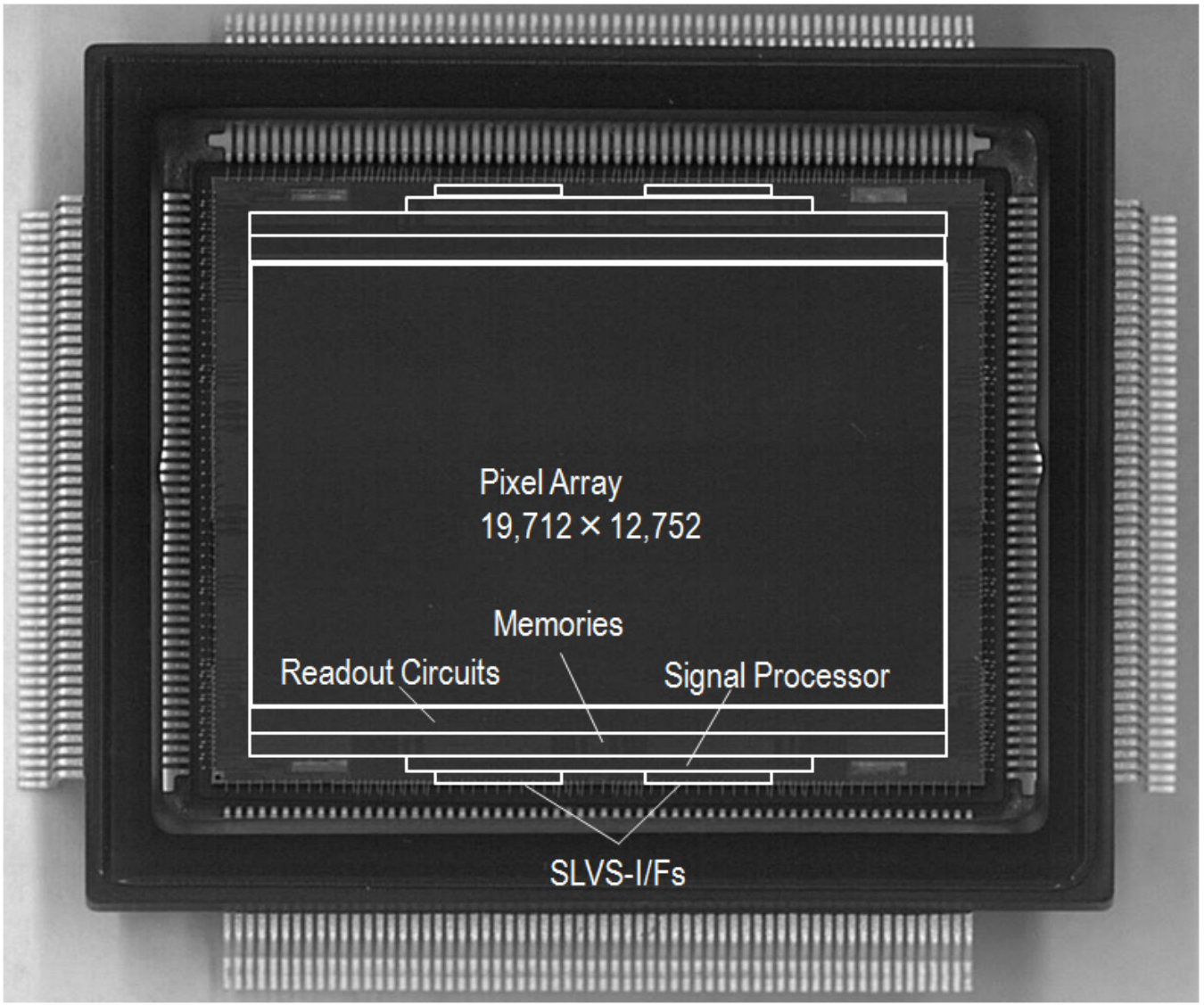
Chip Microphotograph



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Outline

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  - Compensation Process
- ☐ Results
  - Linearity Errors
  - Specifications
  - Image
- ☐ **Summary**

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Summary

- A 250M pixel sensor was developed.

- SSDG-ADC realized the following:

  In comparison with SS-ADC,

  - ~4x faster AD conversion speed
  - Negligible power increase vs. SS-ADC with the amplifiers
    (or 15% power increase vs. SS-ADC without the amplifiers)
  - 6dB wider dynamic range (@ 5fps, full pixel read-out)

- The compensation process suppressed the linearity errors due to SSDG within insignificant level (~±5LSB).

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Thank you very much for your kind attention.

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A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing

M. Perenzoni, D. Perenzoni, and D. Stoppa

FONDAZIONE BRUNO KESSLER

Monday, February 1st – Session 6: **Image Sensors**

Session Chair: *Jun Deguchi, David Stoppa*

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Landing in Space

- Apollo 11 mission on the Moon
- Mars Space Laboratory on Mars
- Rosetta mission on comet 67P/C-G

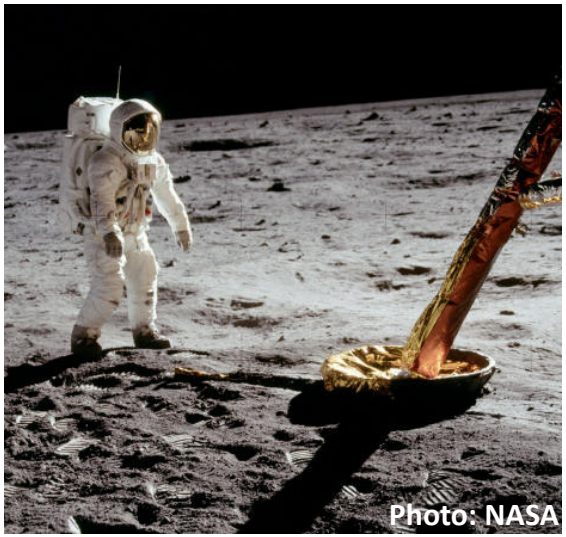
Photo: NASA

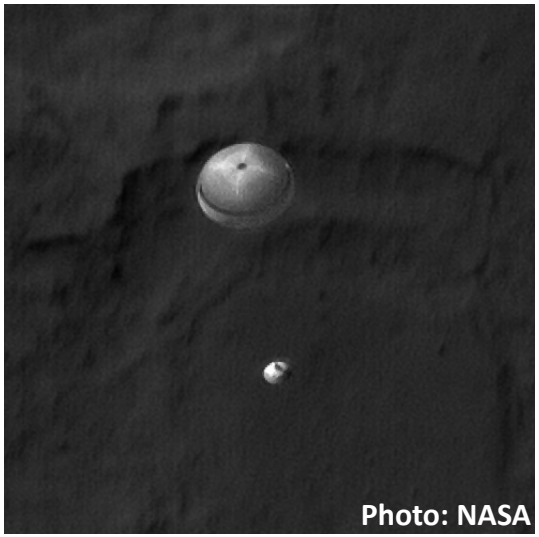
Photo: NASA

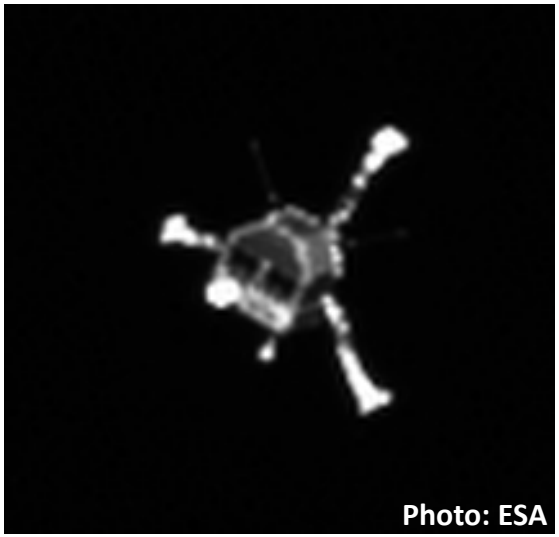
Photo: ESA

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Outline

- The problem
  - Long-range and robust 3D ranging/imaging
- The solution
  - Smart pixel based on d-SiPM
- The results
  - Characterization and 3D images

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Outline

- **The problem**
  - **Long-range and robust 3D ranging/imaging**
- The solution
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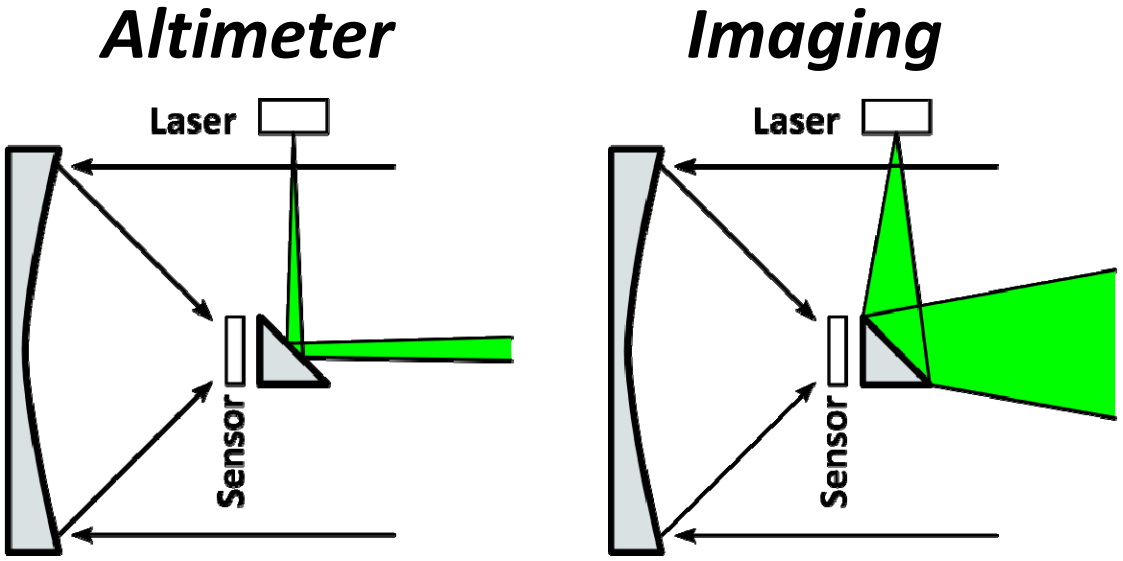
The problem: long-range



• Mode:	100m-6km	30m-300m
• Max ToF:	40µs	2µs
• Precision:	1m (6.6ns)	10cm (660ps)

Wide DR and long light time-of-flight

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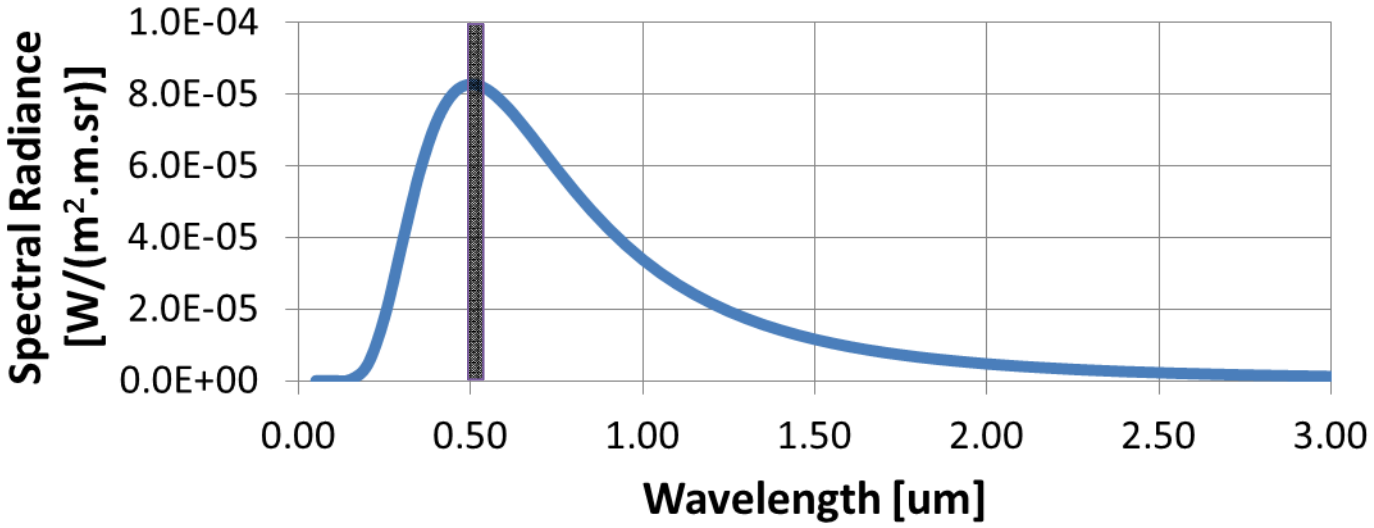
The problem: background



- With targeted pixel size and FF:
  - 100 Mph/s (detected)

5nm filter
Albedo <0.4
Sun angle 30°

High Background Rejection

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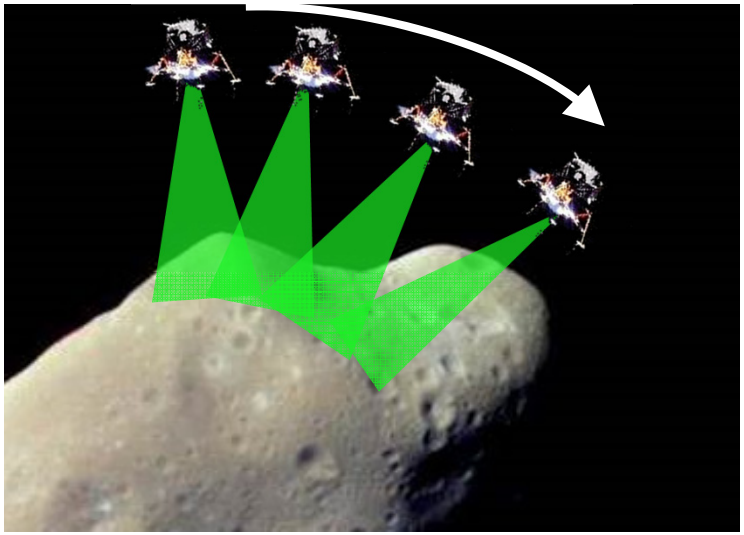
The problem: speed



Spacecraft speed:
0.1 m/s - 1.5 m/s

- No artifacts within 1 pixel
  - Fast image acquisition < 2 ms
  - Low frame rate ≈ 2 fps

} ***Enabling post-processing***

Short Acquisition Time

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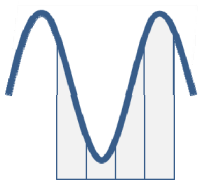
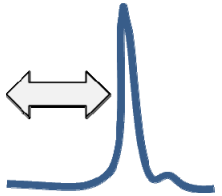
Ranging Techniques



TOF



Indirect TOF

- Long integration time ☹
- Ambiguity ☹
- Analog dynamic range 😐
- Large no. of pixels ☺

Direct TOF

- ☺ Fast acquisition
- ☺ No ambiguity
- ☺ Digital dynamic range
- ☹ Reduced no. of pixels

Challenge: single-photon detectors are bg sensitive and noisy

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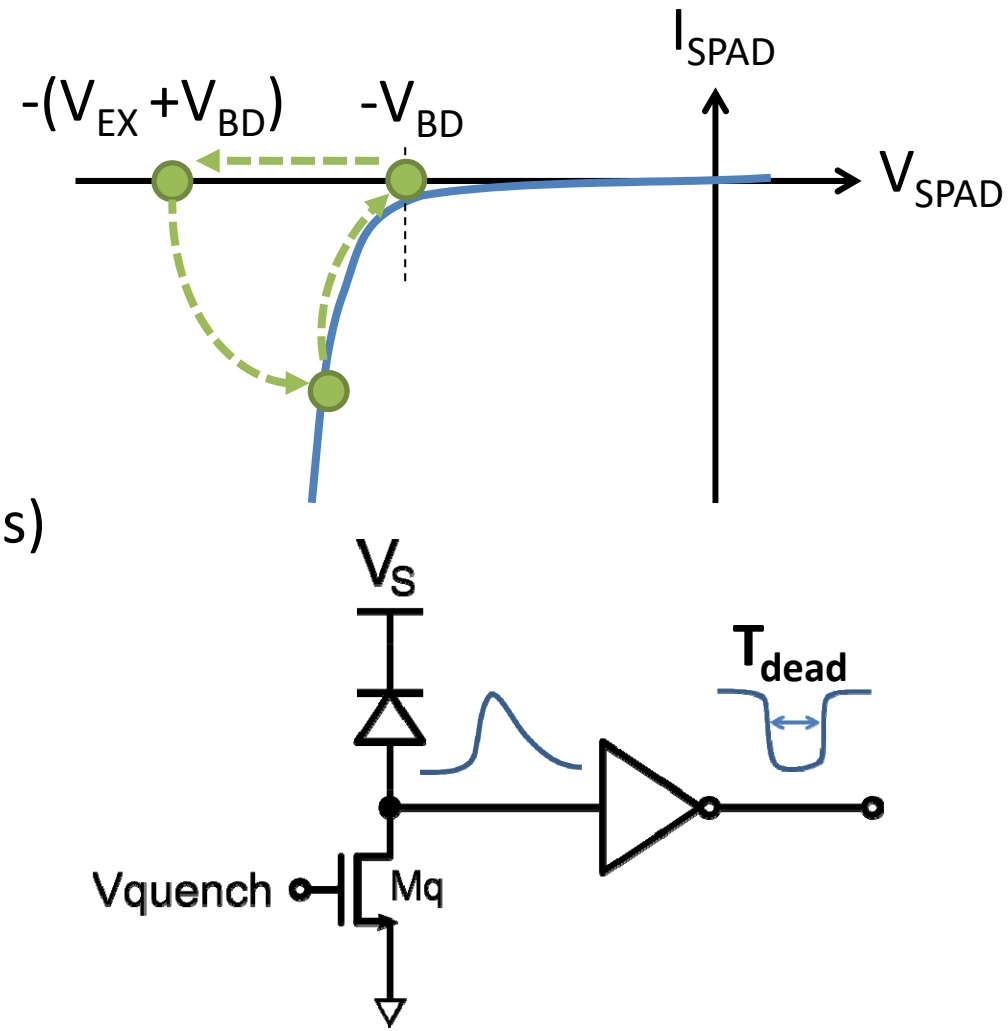
Single-Photon Avalanche Diodes

- SPAD operation
  - Avalanche
    - Triggered by
      - Photons
      - Noise (dark counts)
  - Quenching
  - Recharge



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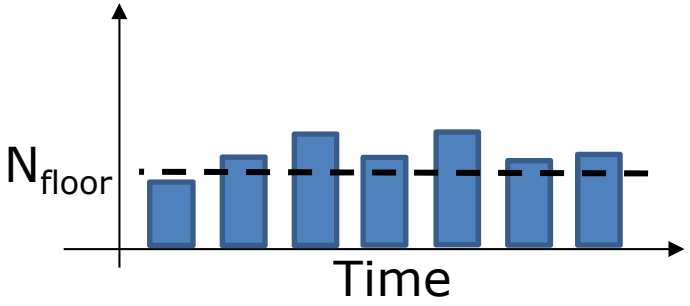
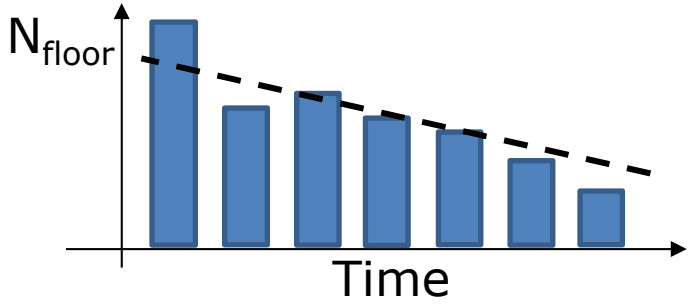
Pile-up and Strong Flux

- **SPAD** ➡ deadtime 
- **Stopwatch** ➡ memory 

$$N_{floor\,0} = N_a T_{BIN}\left(DCR + f_{bg}\right) \qquad N_{floor}(t) \approx N_{floor\,0} \cdot e^{-\left(DCR + f_{bg}\right)t}$$



No pile-up
(low event rate)



Pile-up
(high event rate)

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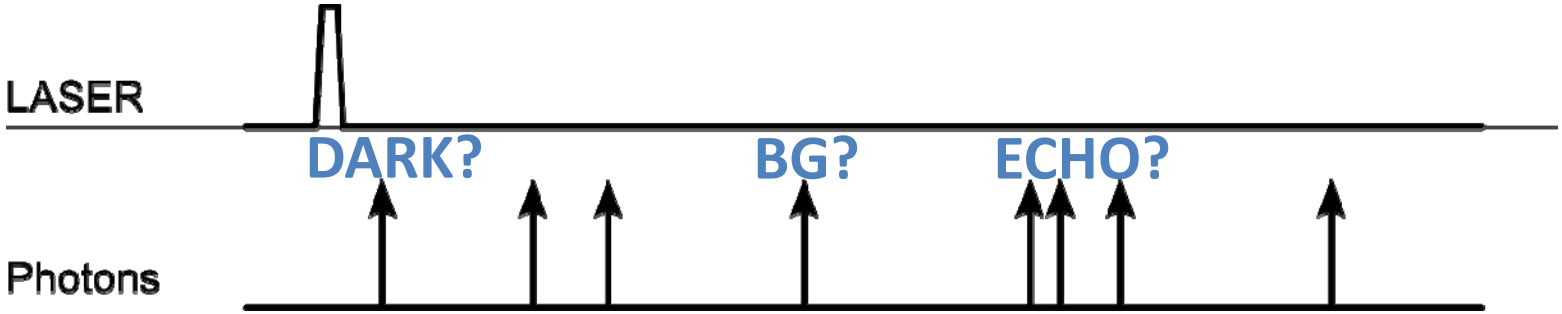
Previous Solutions Limitations

- **Single SPAD + TDC** [Veerappan, ISSCC 2011]
  - Compact pixel (but low FF) ☺
  - First event (dark, bg, echo…): TDC timestamp ☹



- **Multiple SPAD + TDC** [Niclass, JSSC 2014]
  - First relevant event captured ☺
  - Few pixels, imaging through scanning ☹

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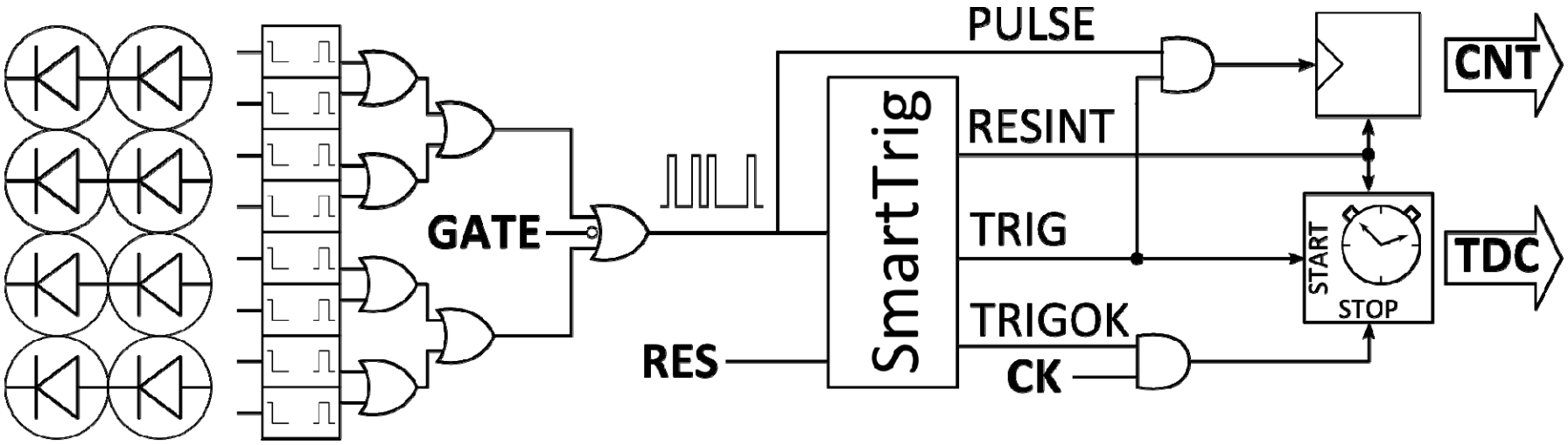
Pixel Schematic



Digital SiPM

Smaller deadtime

Triggering Logic

Identify echo

Counter & TDC

Timestamp and count

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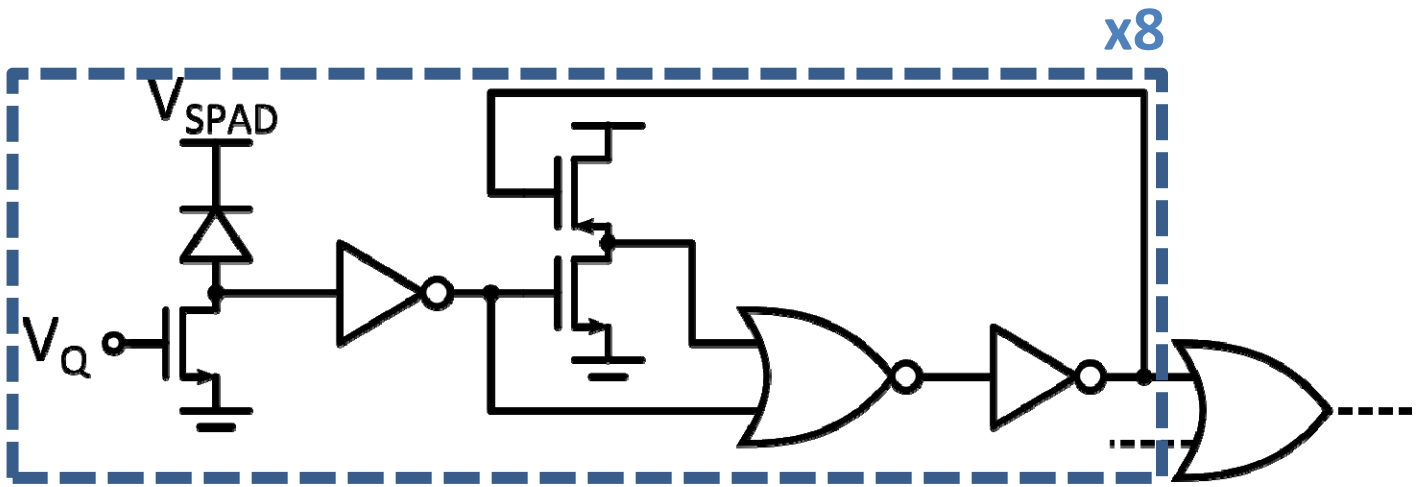
8-SPAD Digital SiPM

- Passive quenching
- Feedback-based monostable
- OR-tree: NAND-NOR combination



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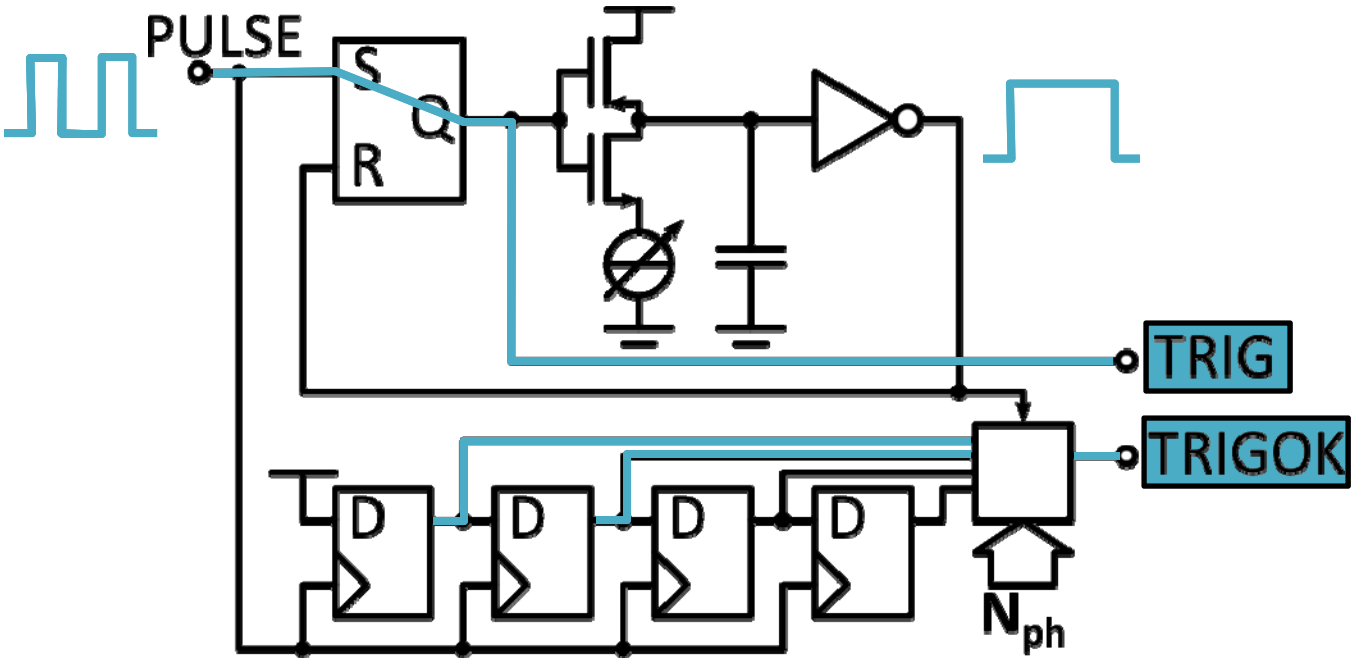
Smart Triggering Logic

- Immediate trigger out (to TDC)
- Validate or restart



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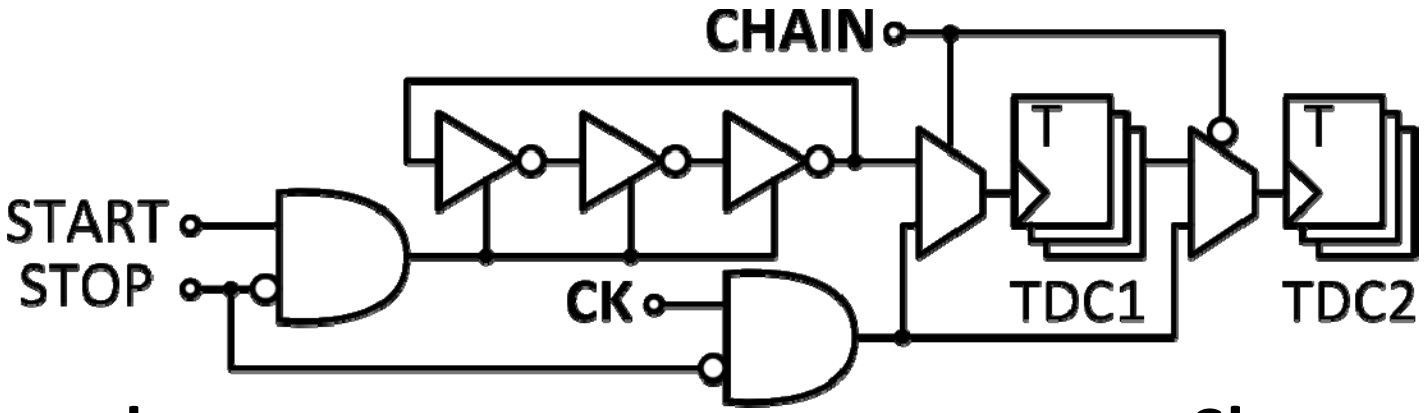
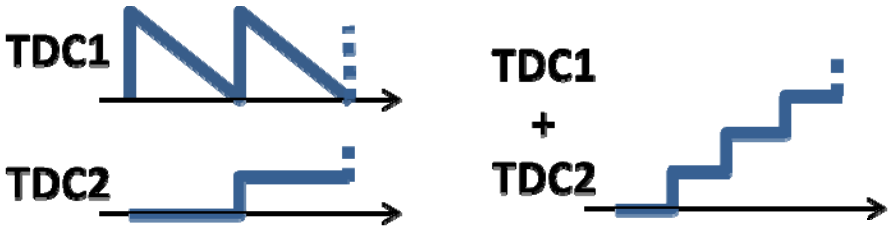
Counter and TDC

- 4-bit ripple counter
- Ring oscillator/clock TDC: dual operation



Fast mode: R-O plus CK counter (LSB≈250ps)



Slow mode: chained CK Counter (LSB≈10ns)

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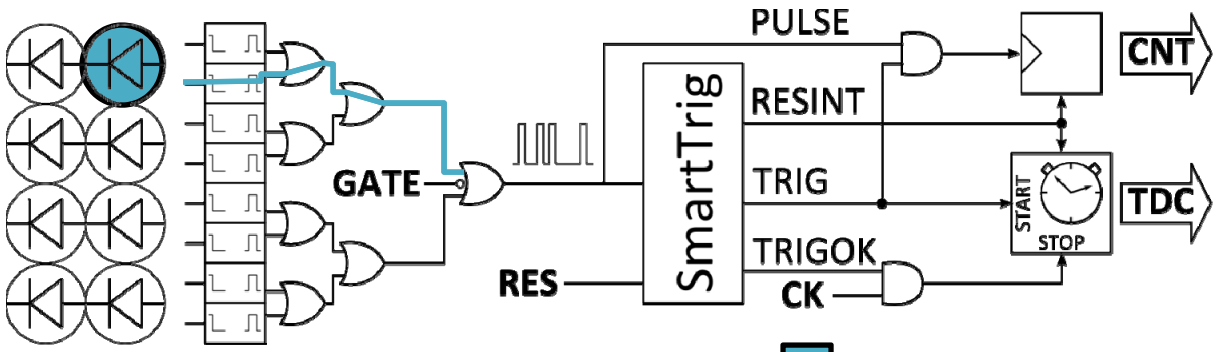
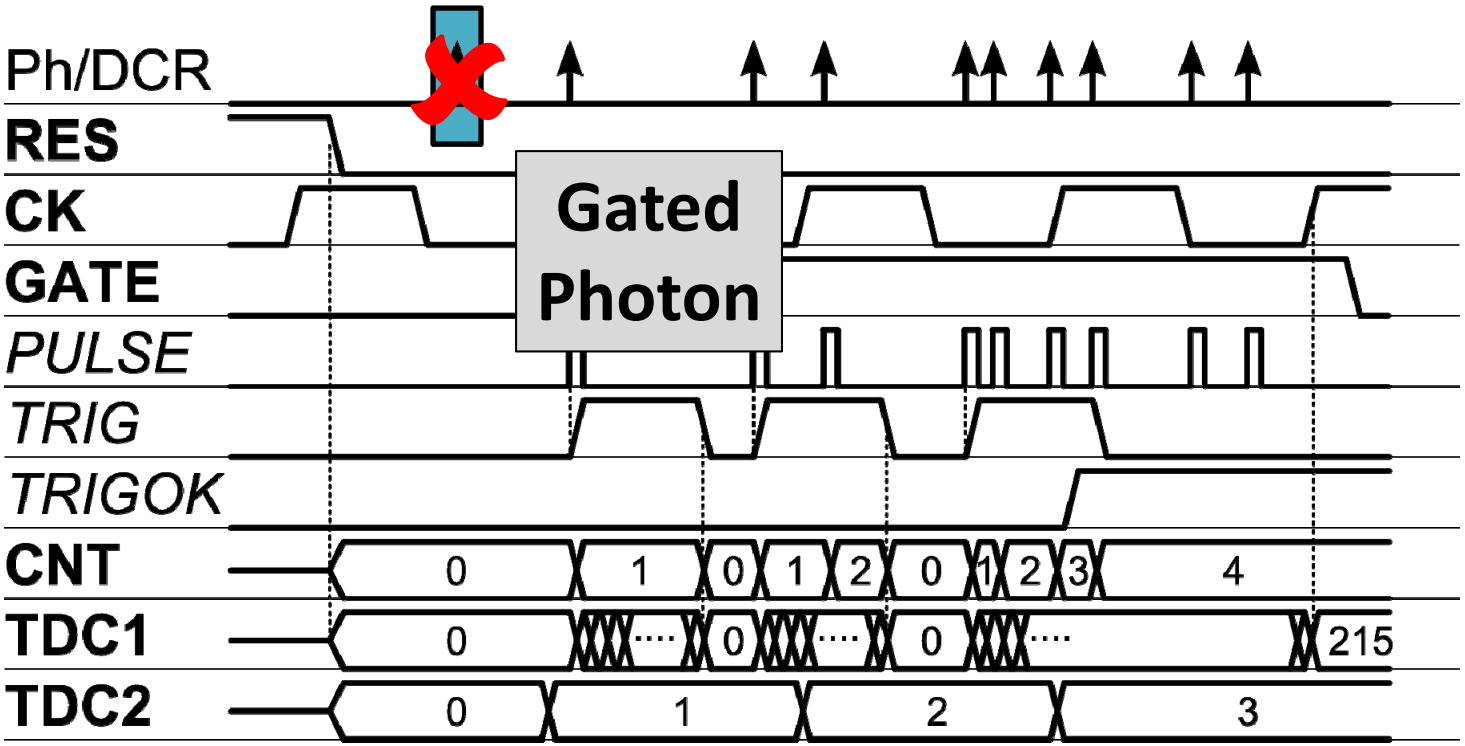
Detailed Operation





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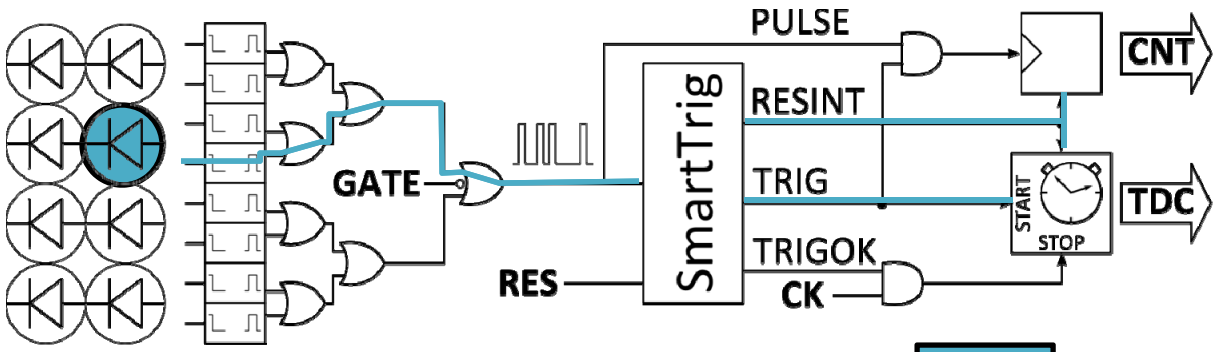
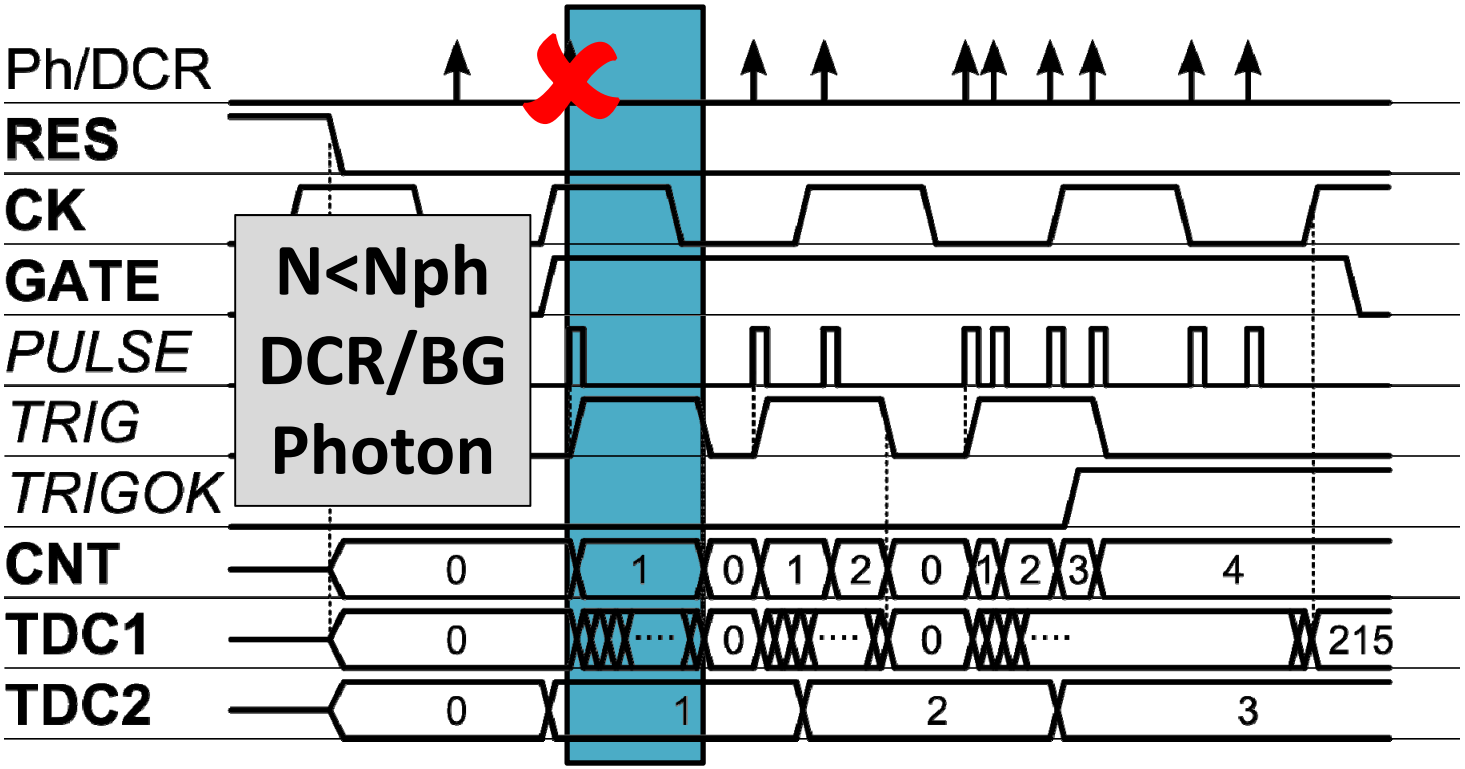
Detailed Operation





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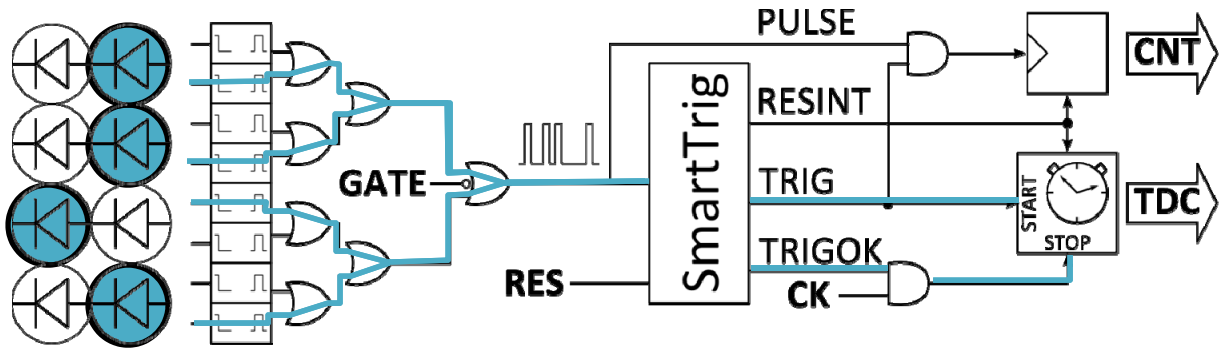
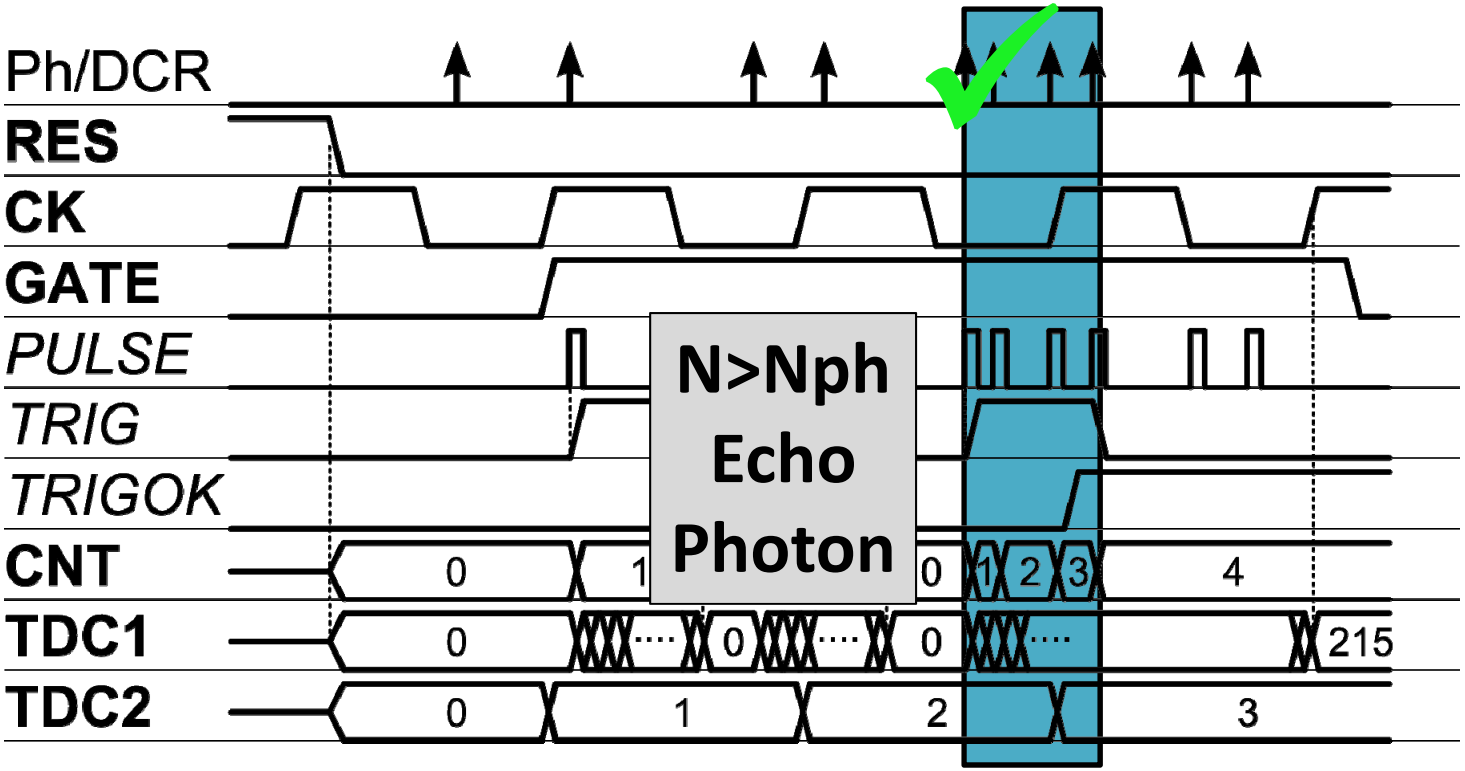
Detailed Operation





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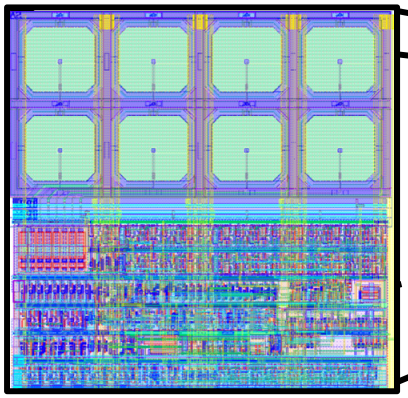
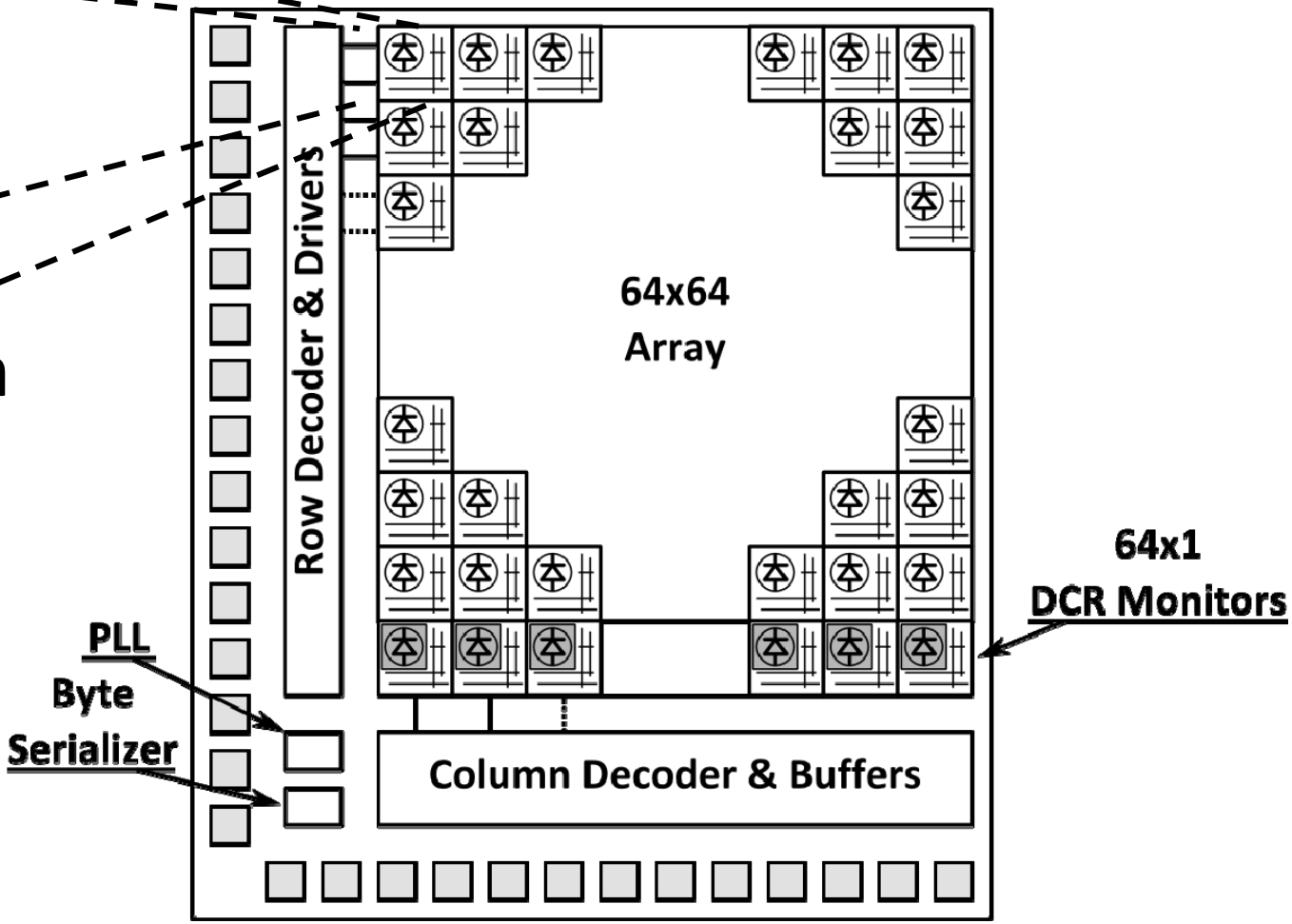
Chip Architecture





- 60-µm pitch
- 26.5% FF
- 16-bit TDC
  - LSB 250ps
  - PLL-locked
- 4-bit CNT

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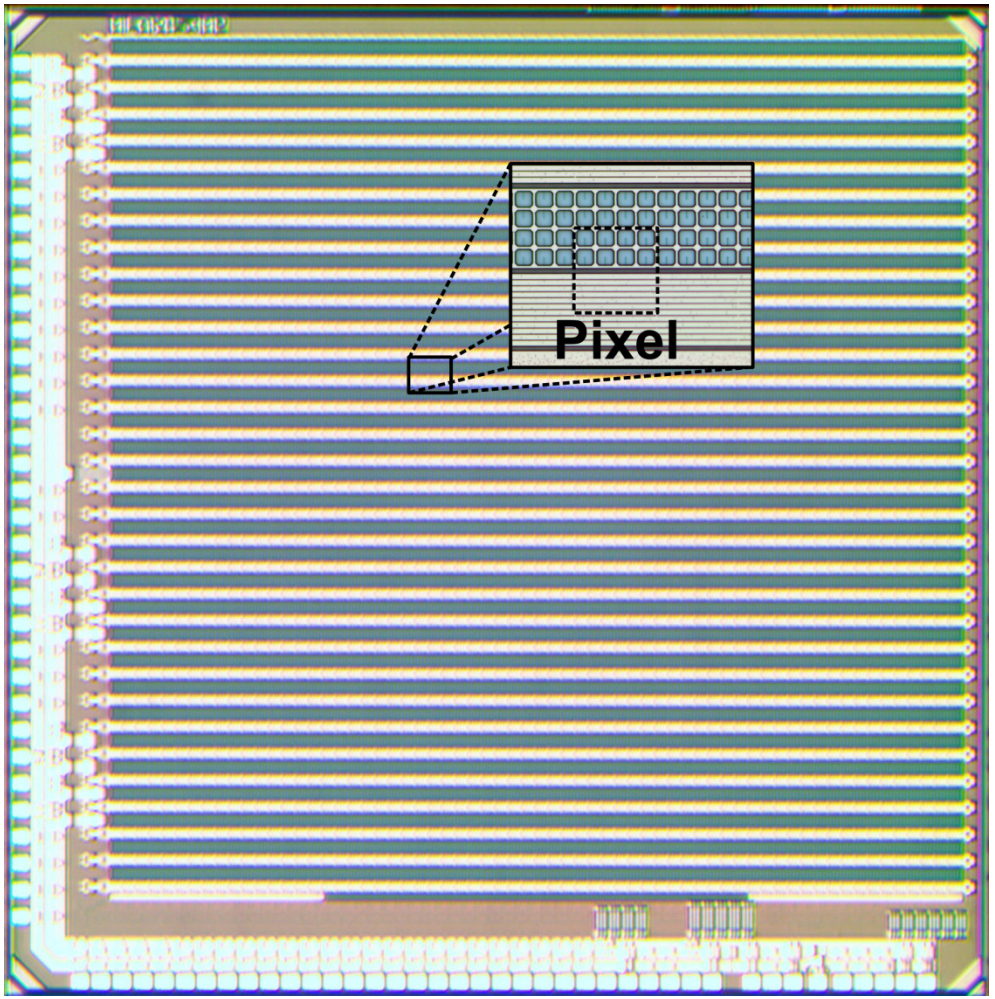
Chip Micrograph

- 150nm CMOS
- 4.4×4.4mm^2
- P_{el} = 47.7mW
- P_{SPAD} = 45.8mW
- 1920 fps



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Outline

- The problem
  - Long-range and robust 3D ranging/imaging
- The solution
  - Smart pixel based on d-SiPM
- **The results**
  - **Characterization and 3D images**

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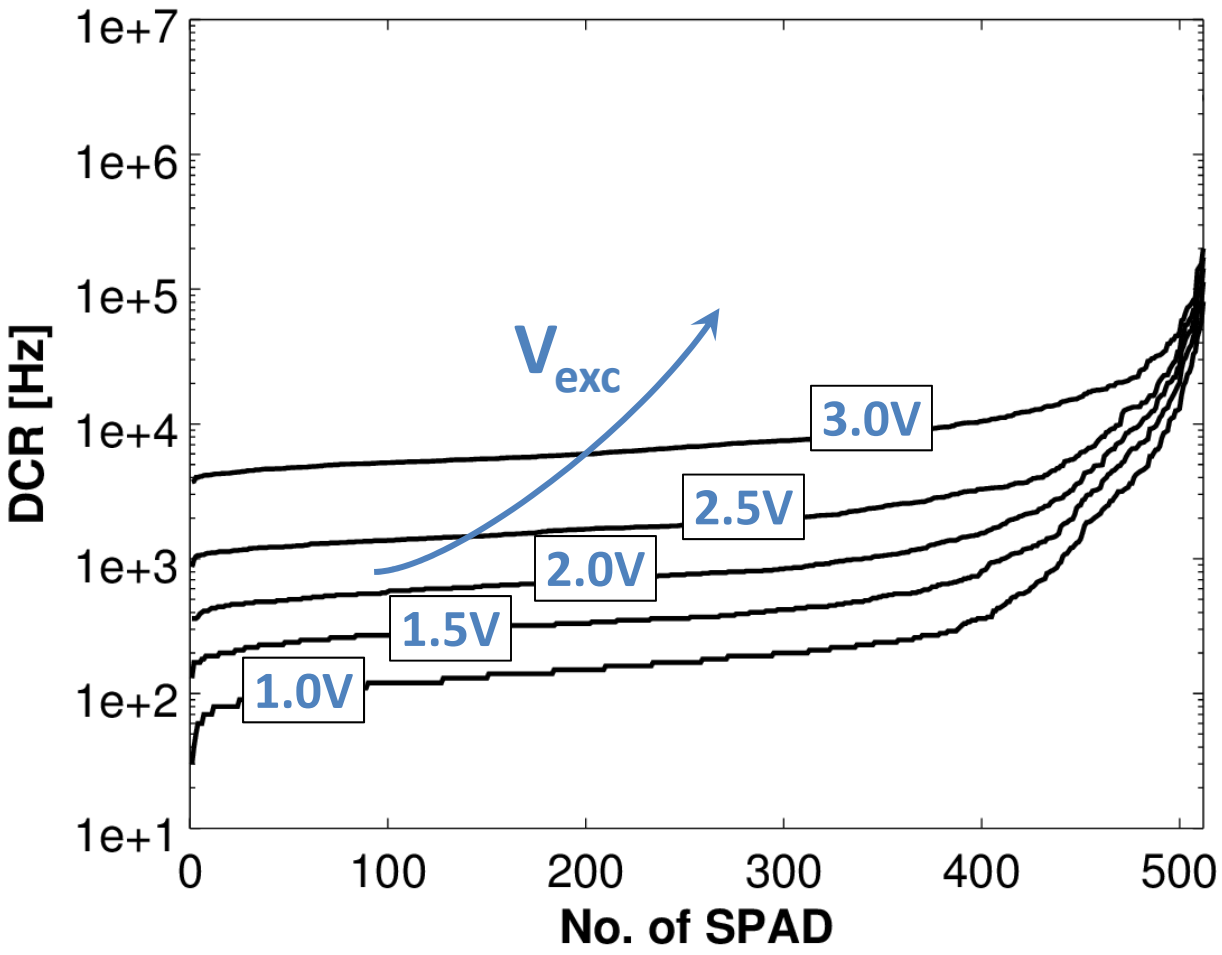
SPAD Characterization



- SPAD
  - P+/N-
  - 11×11μm²
- DCR Monitors
  - 8 SPAD/pix
  - 64 pix
- Median DCR
  - 6.8kHz@3V

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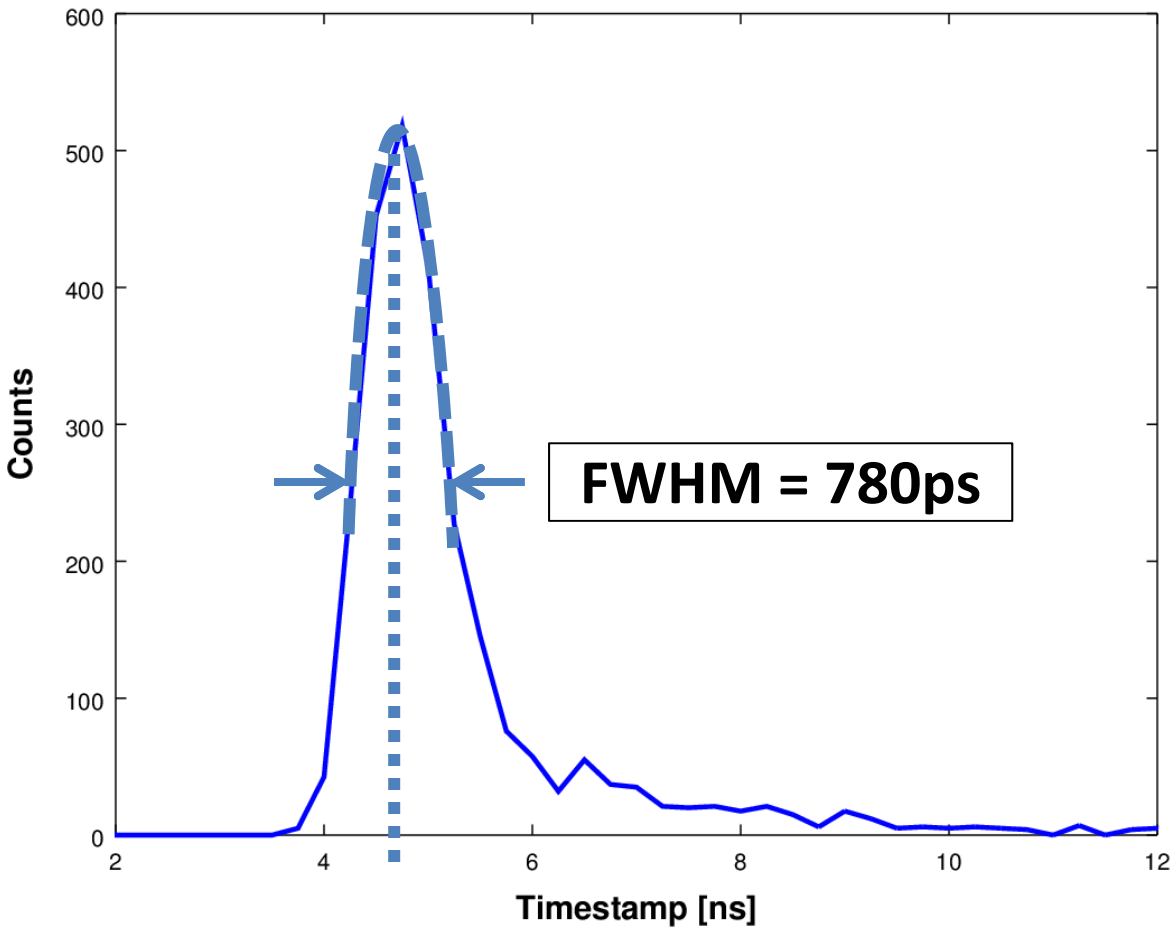
Timing Resolution



- Conditions:
  - 70-ps Laser (attenuated)
  - 5000 frames
  - Single pixel
  - 250-ps LSB

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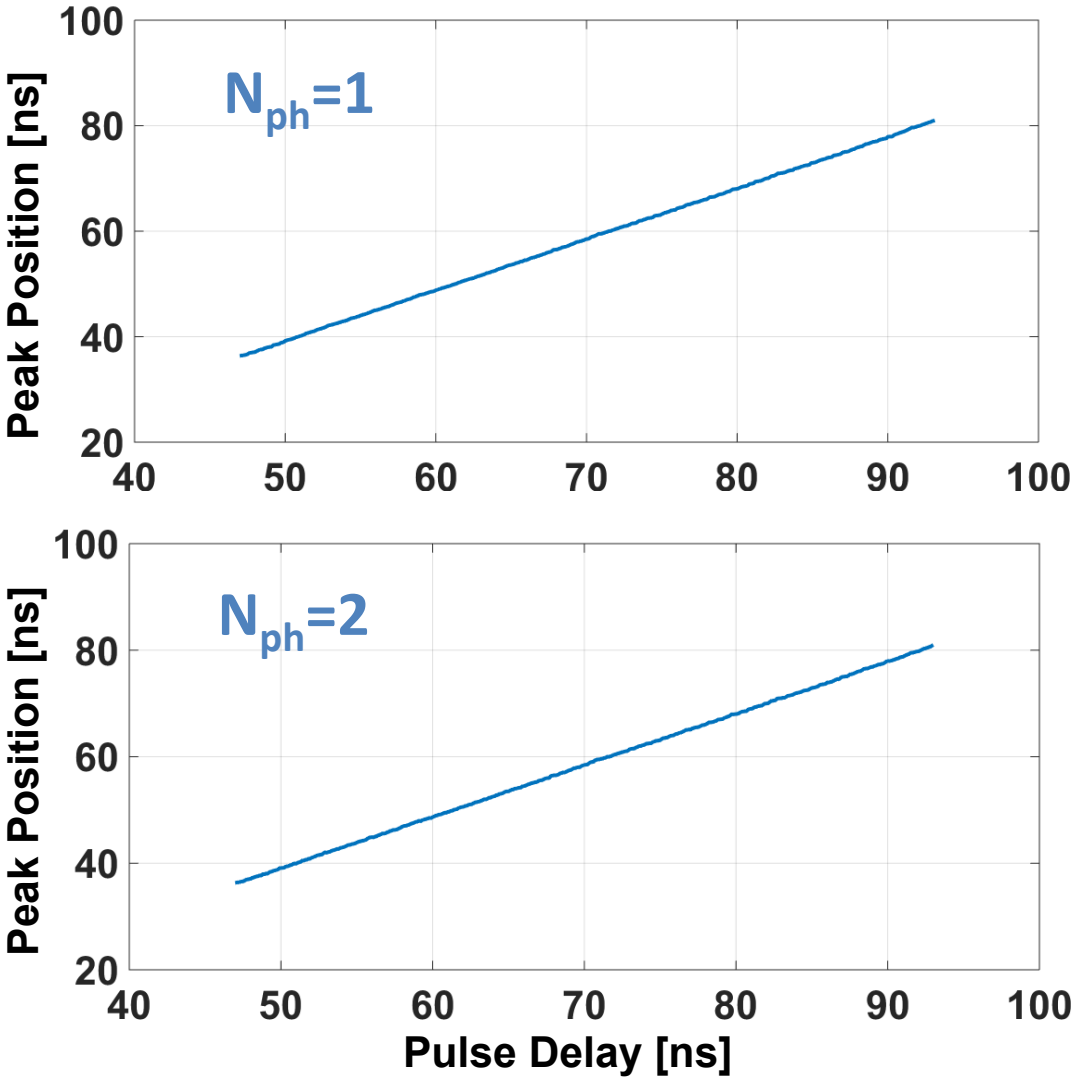
Distance (Time) Sweep



- Conditions:
  - 70-ps Laser (attenuated)
  - Sweep delay
  - 13x13 pixels
  - Pulse centroid
  - T_{CK} = 40ns
    - LSB: 250ps

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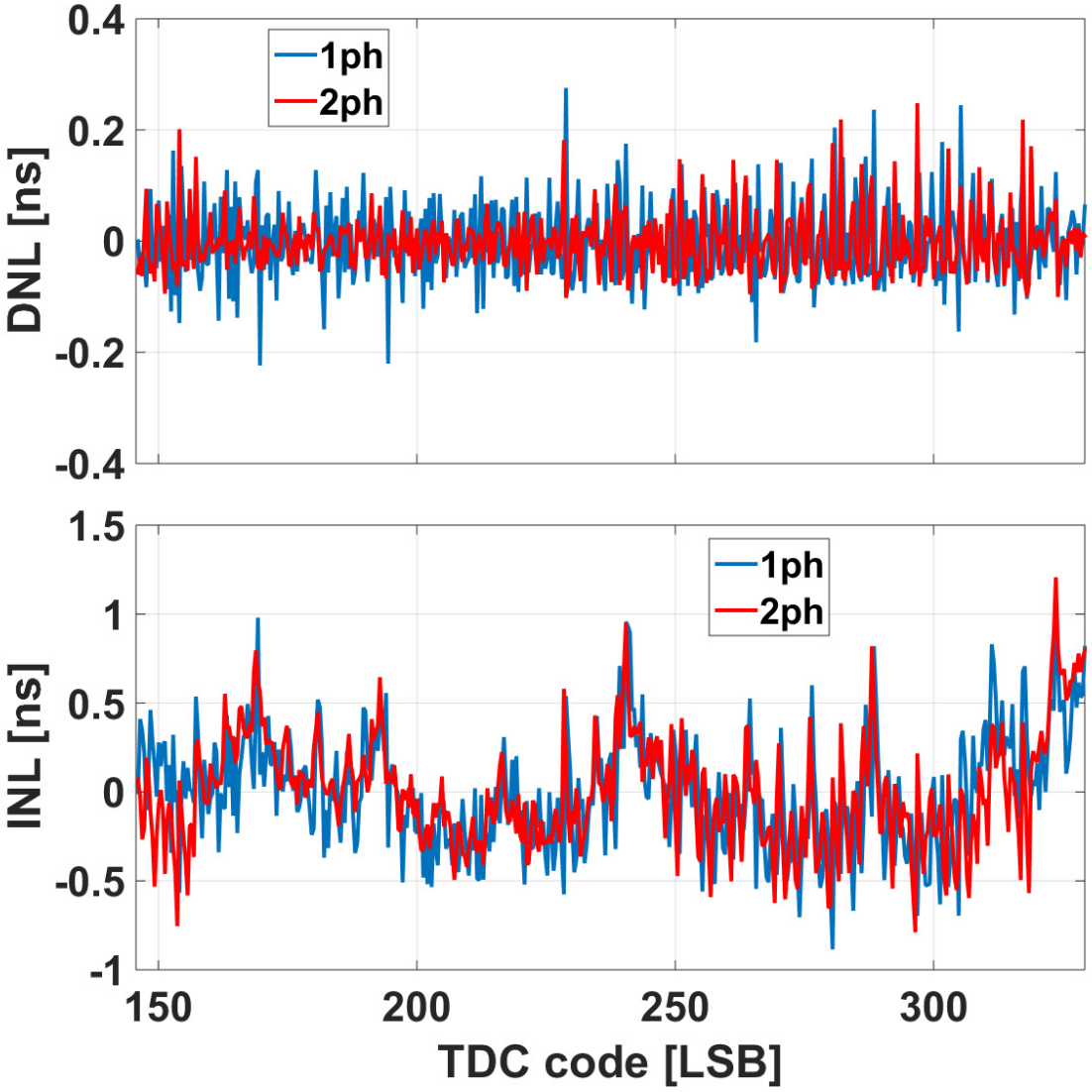
Distance (Time) Linearity



- Conditions:
  - 70-ps Laser (attenuated)
  - Sweep delay
  - 13x13 pixels
  - Pulse centroid
  - T_{CK} = 40ns
    - LSB: 250ps

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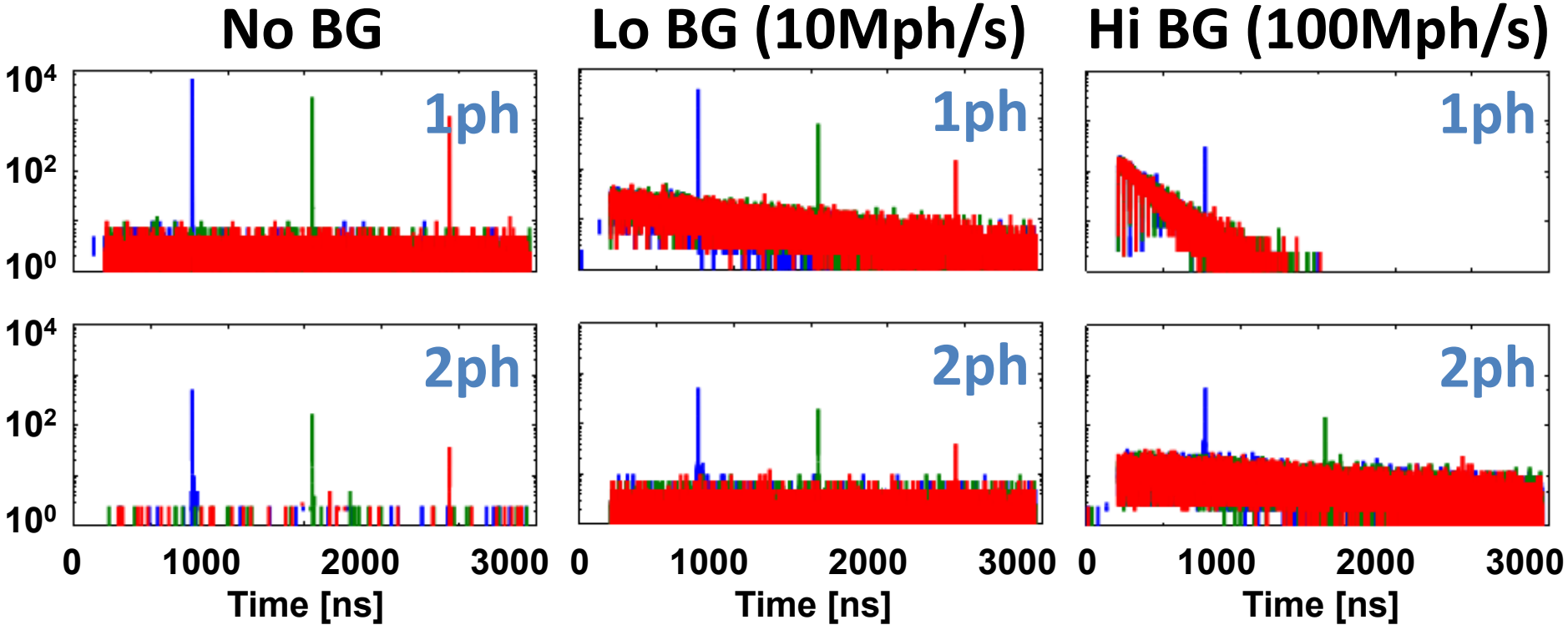
Pile-up With Smart Trigger



- Strong background/DCR is rejected
- Smaller laser peaks

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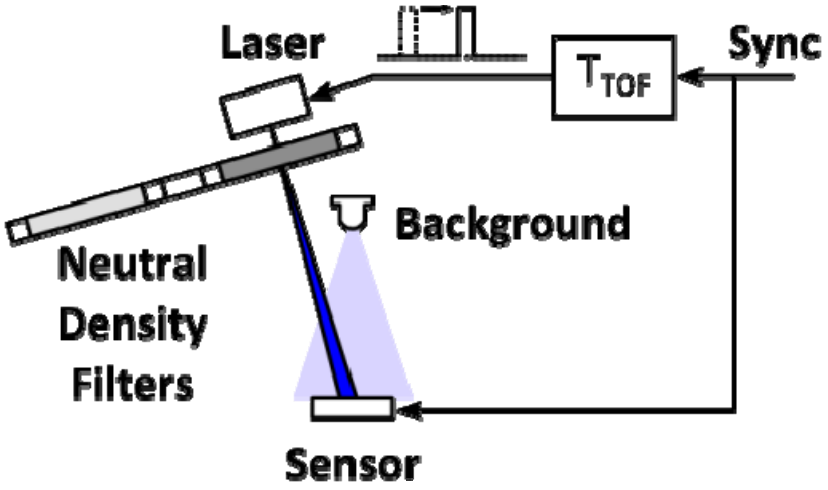
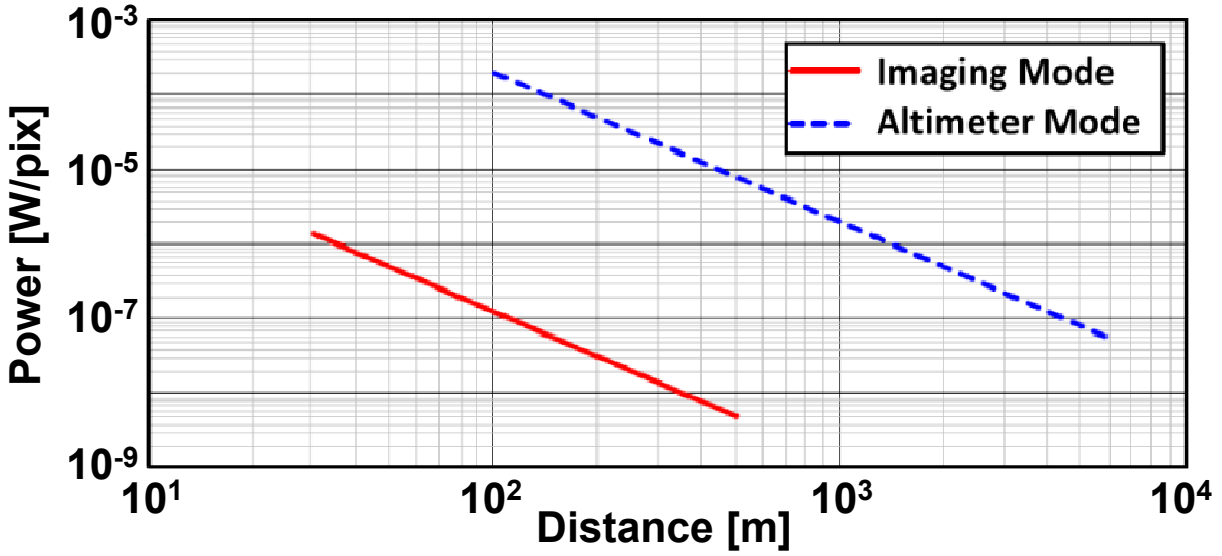
Real Conditions: Range Emulation

- Test vehicle conditions:
  - Laser: P_{pk}=7.5kW
  - 50% albedo
  - 2x2 sensors
  - F#=0.8
- 250-pts acq





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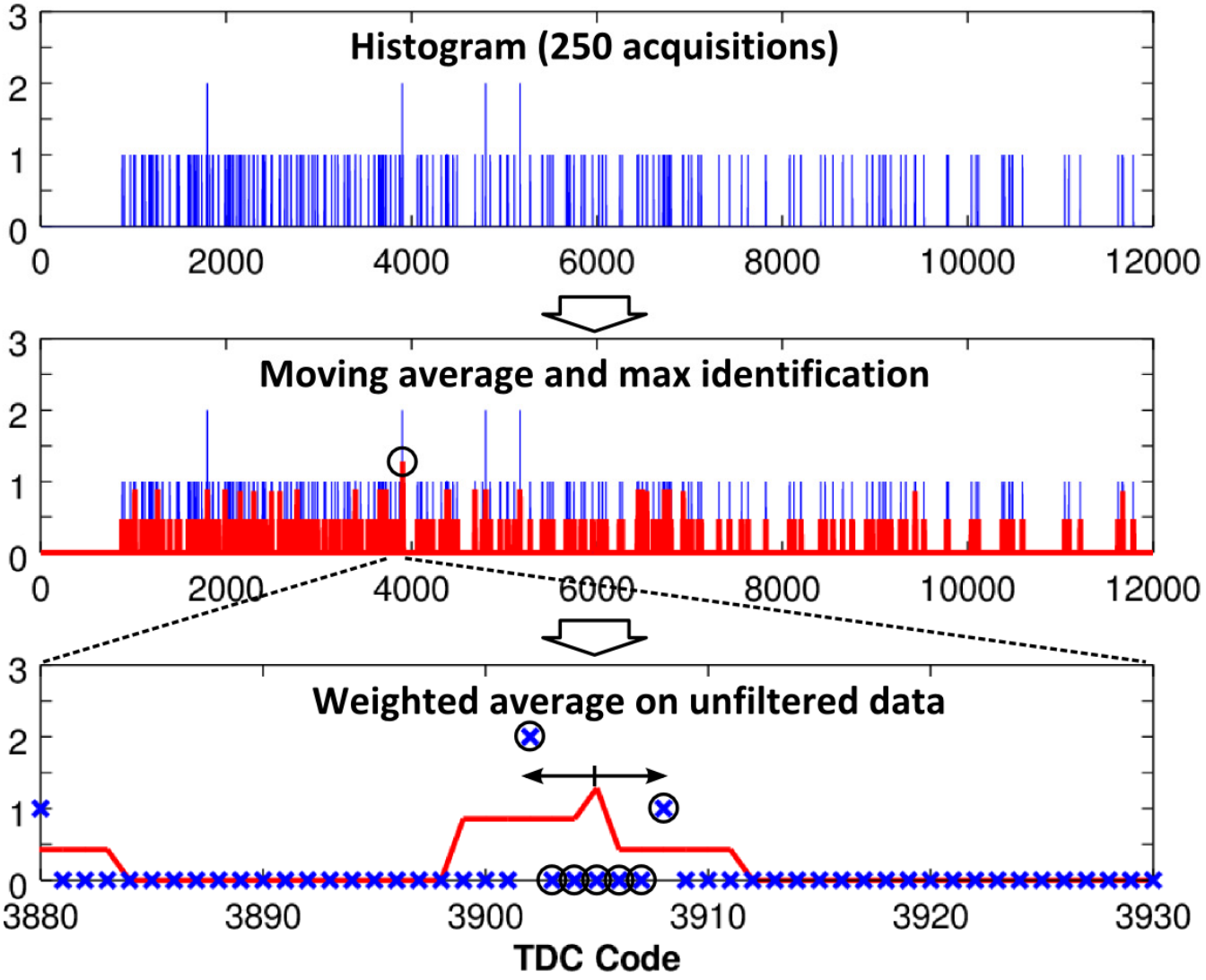
How a 250-pts Histo Looks Like?



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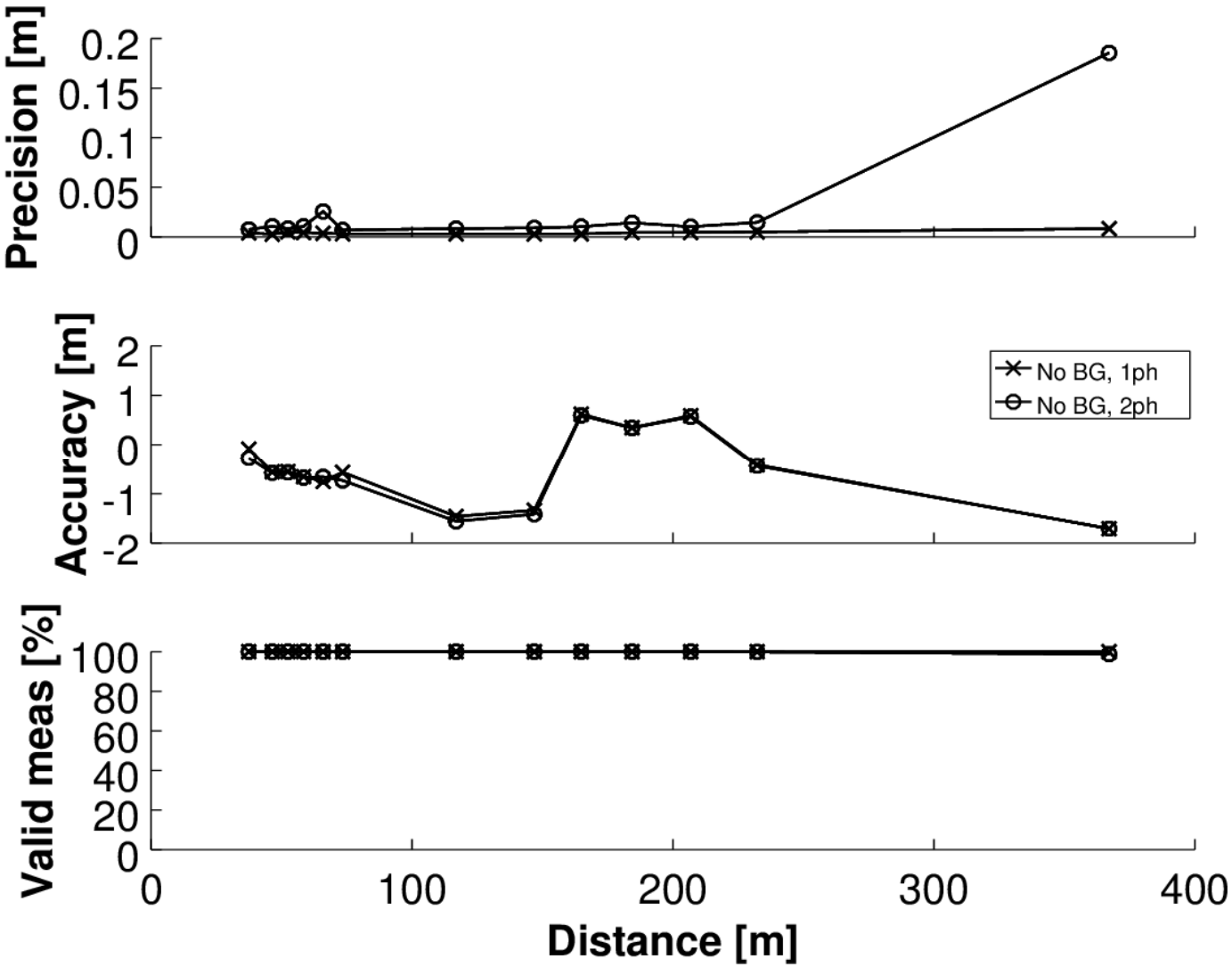
Imaging, no BG



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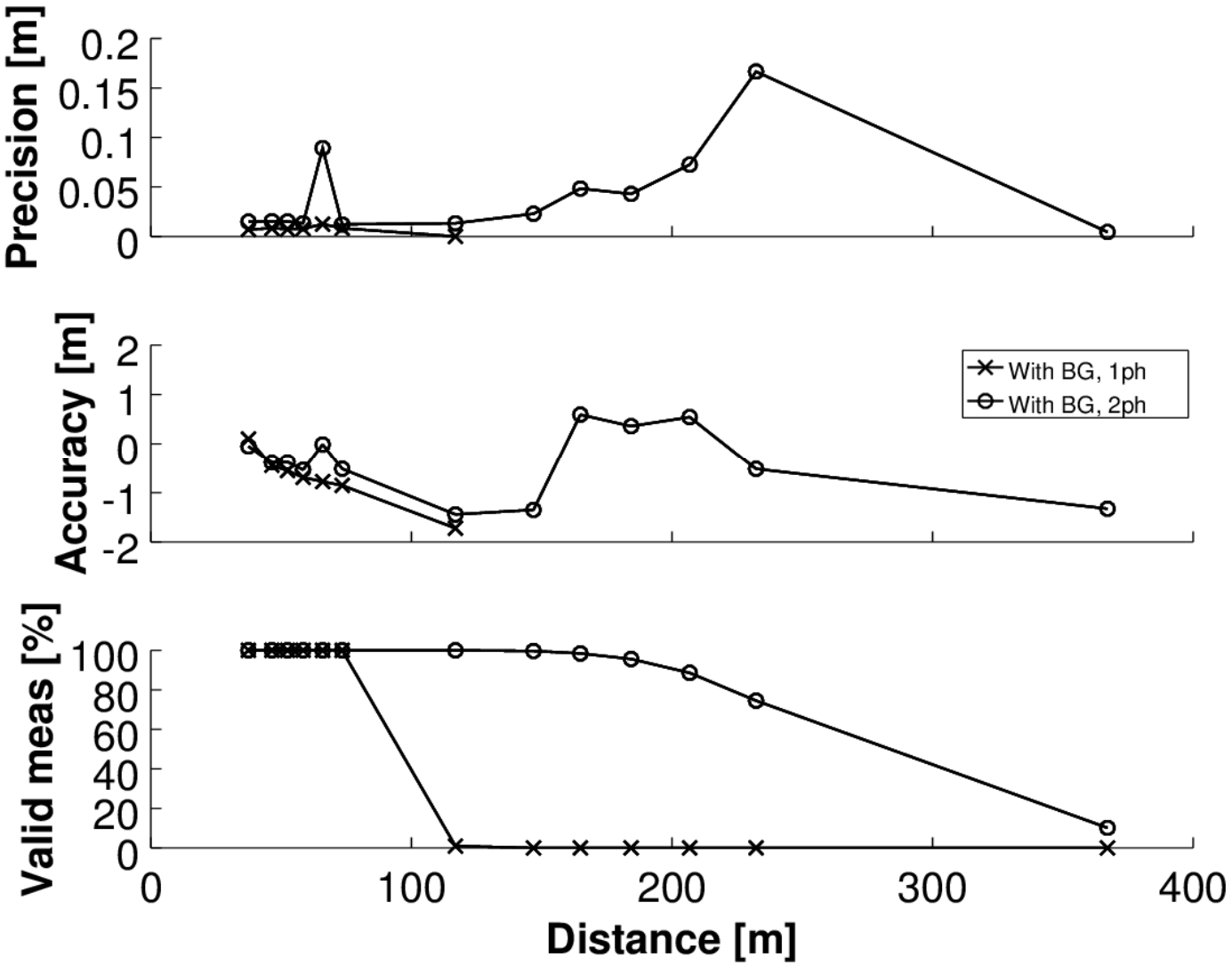
Imaging, BG



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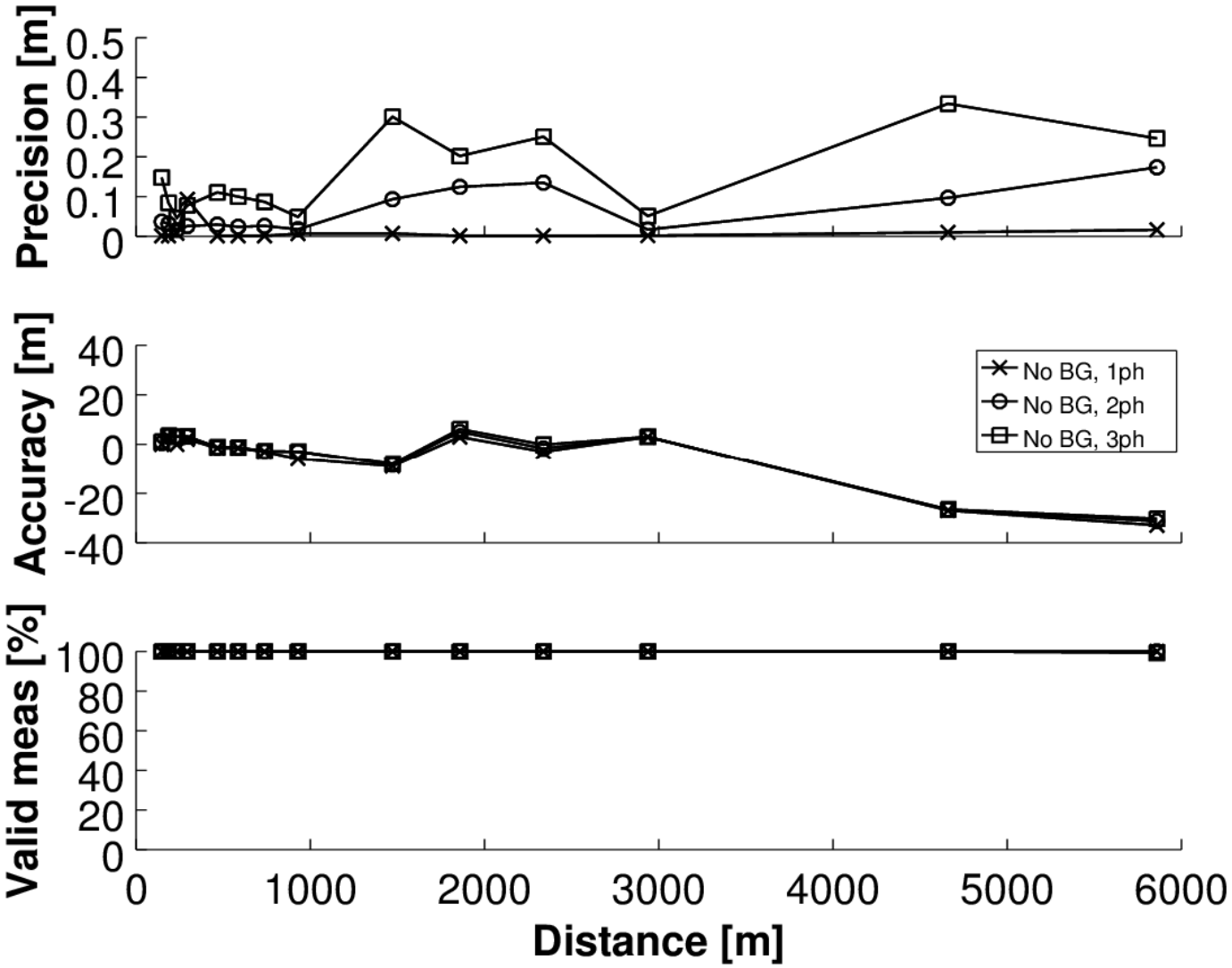
Altimeter, no BG



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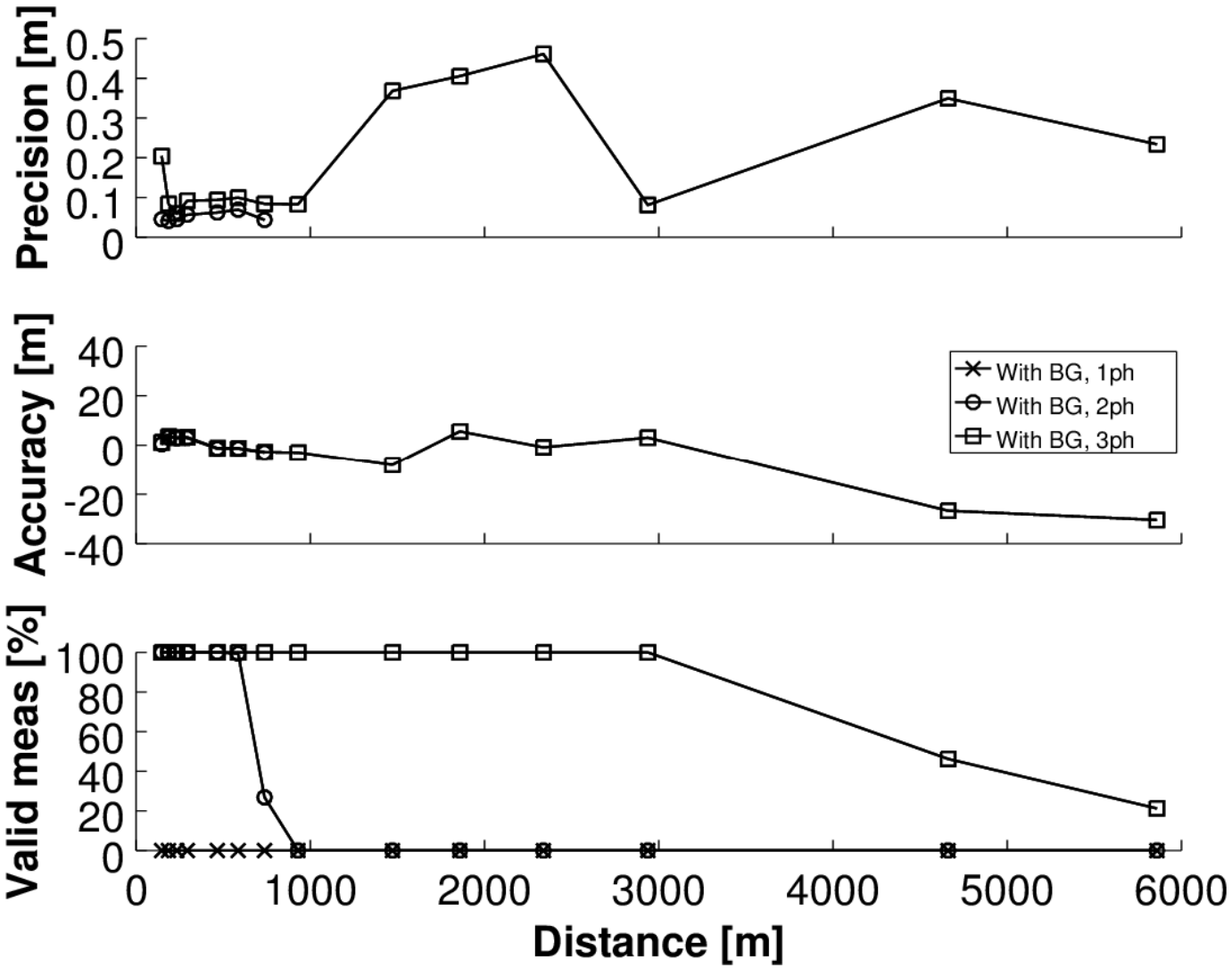
Altimeter, BG



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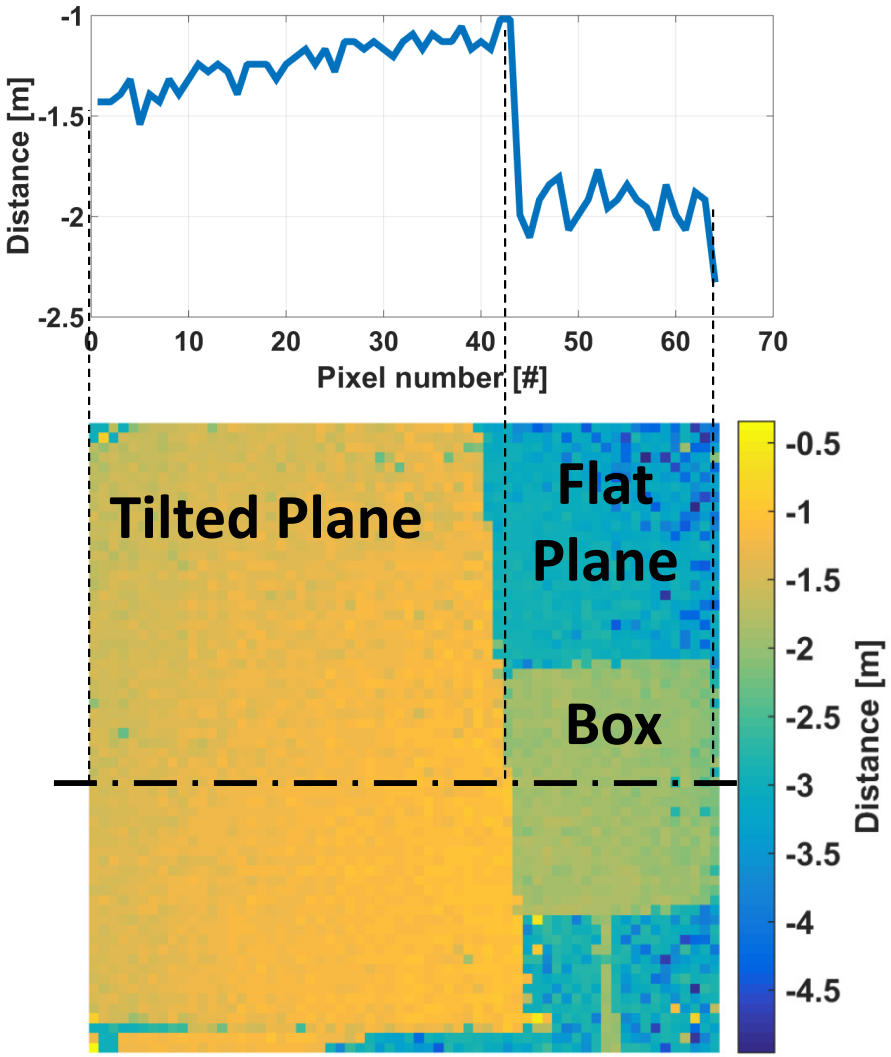
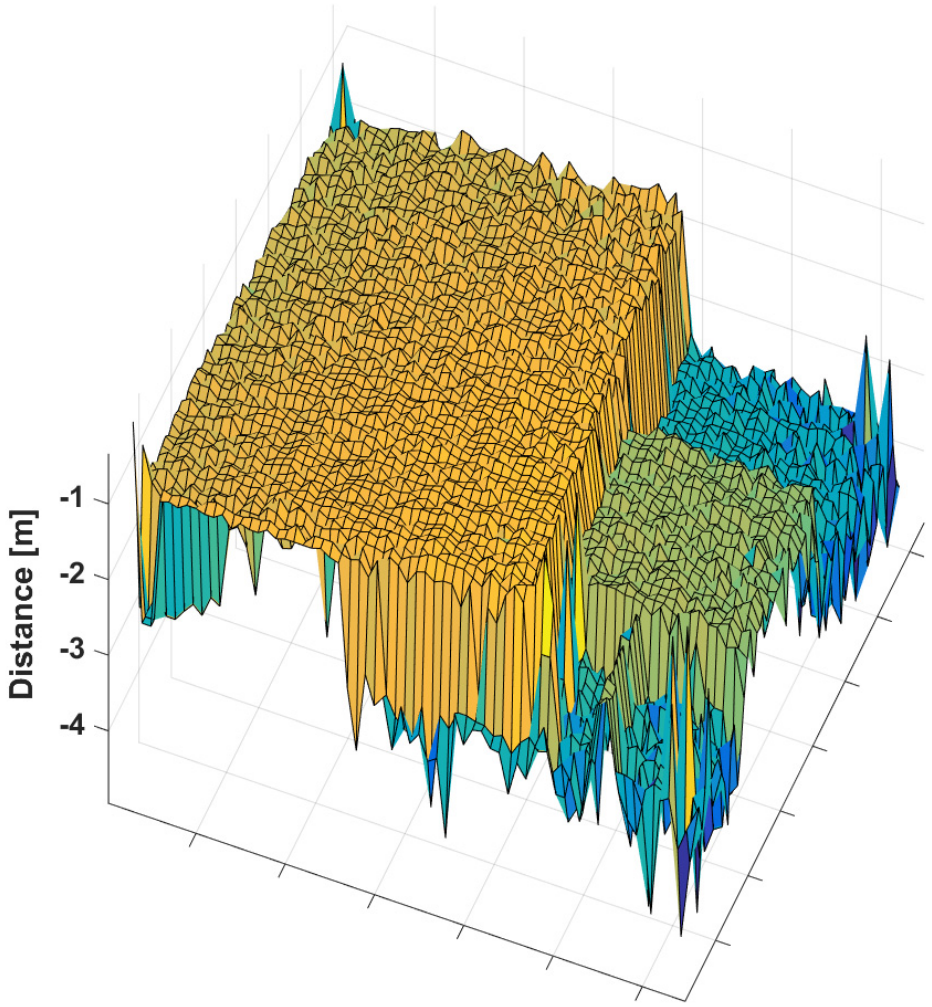
Short-Range 3D Imaging (2ph)





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Conclusions

- We developed
  - Imager with d-SiPM based pixel
  - Per-pixel multiple photon time correlation
  - Improved dark/BG counts rejection
- Future developments
  - Imaging altimeter breadboard
  - Irradiation tests
  - Larger sensor

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Thank you!

DS1

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A 1280×720 single photon detecting image sensor with 100dB dynamic range using a sensitivity boosting technique

M. Mori, Y. Sakata, M. Usuda, S. Yamahira,
S. Kasuga, Y. Hirose, Y. Kato, T. Tanaka

Panasonic Corporation, Japan

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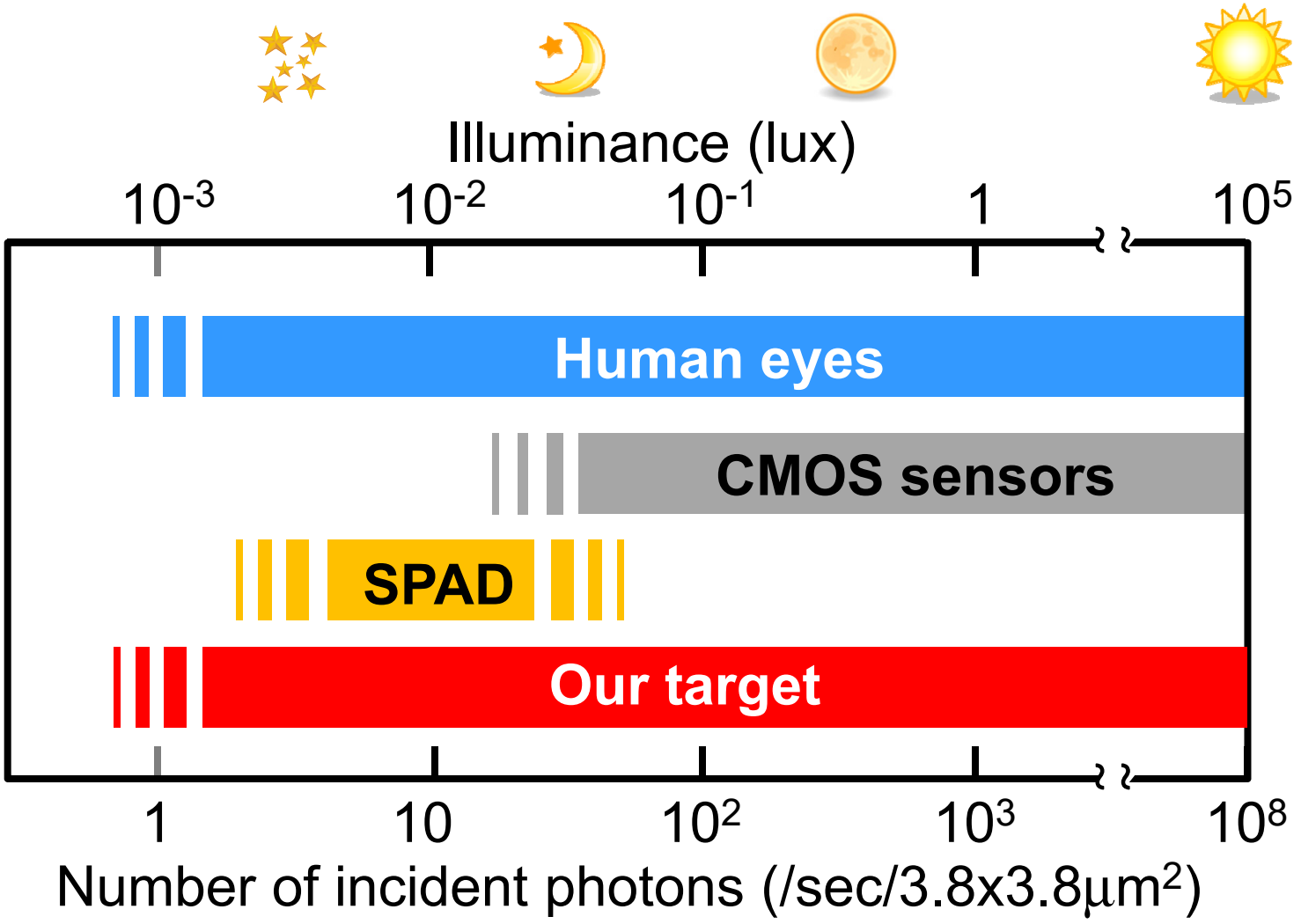
Motivation

Clear digital imaging toward human eyes



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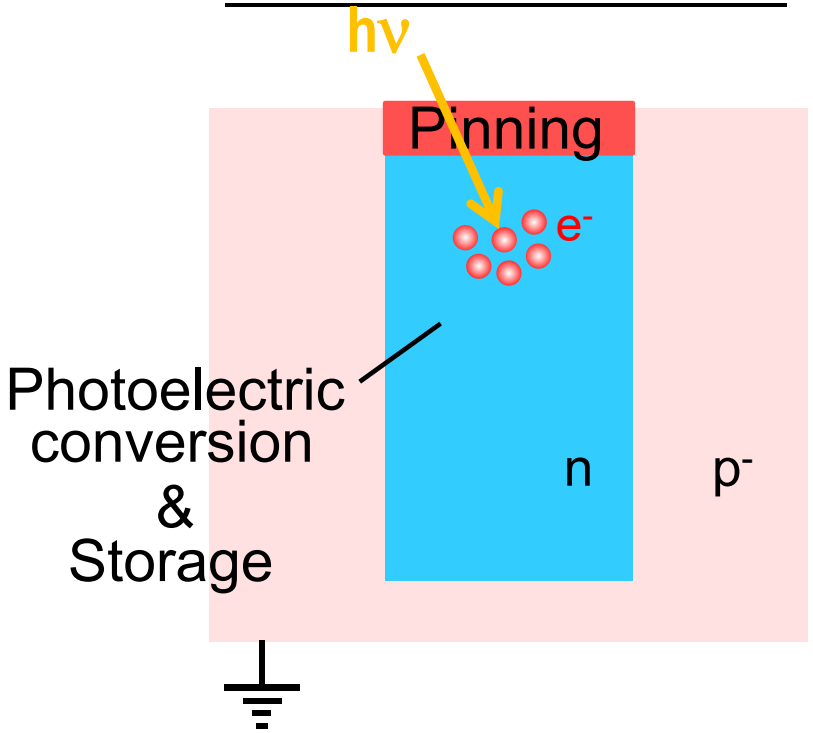
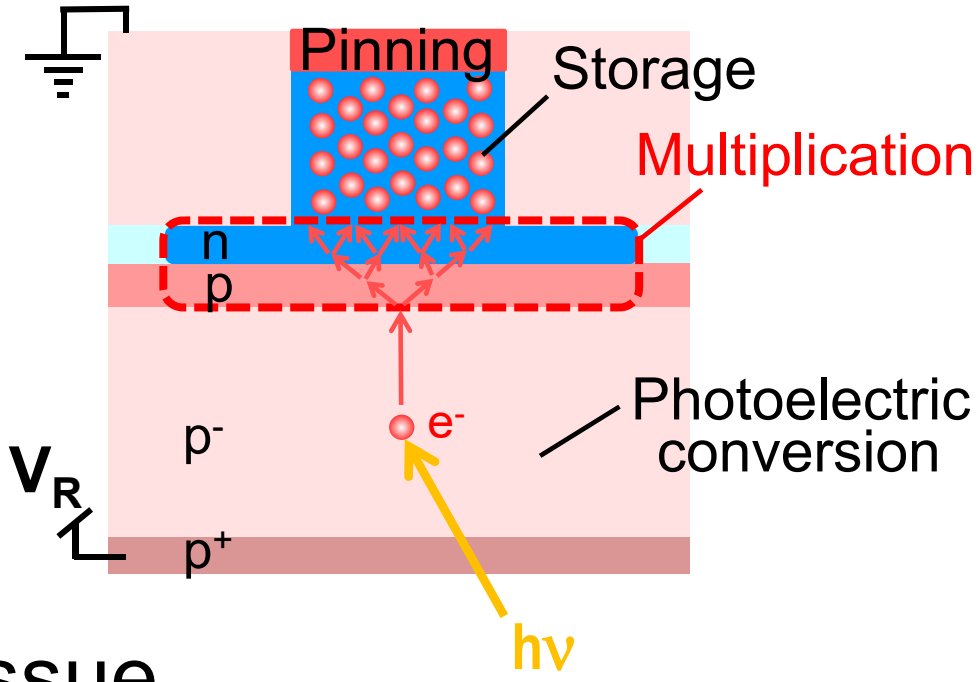
Challenge to Single-Photon Detection

Multiplying photoelectrons before readout

Conventional PD



This work



Issue

APD insertion and isolating Tr.-region from high-voltage

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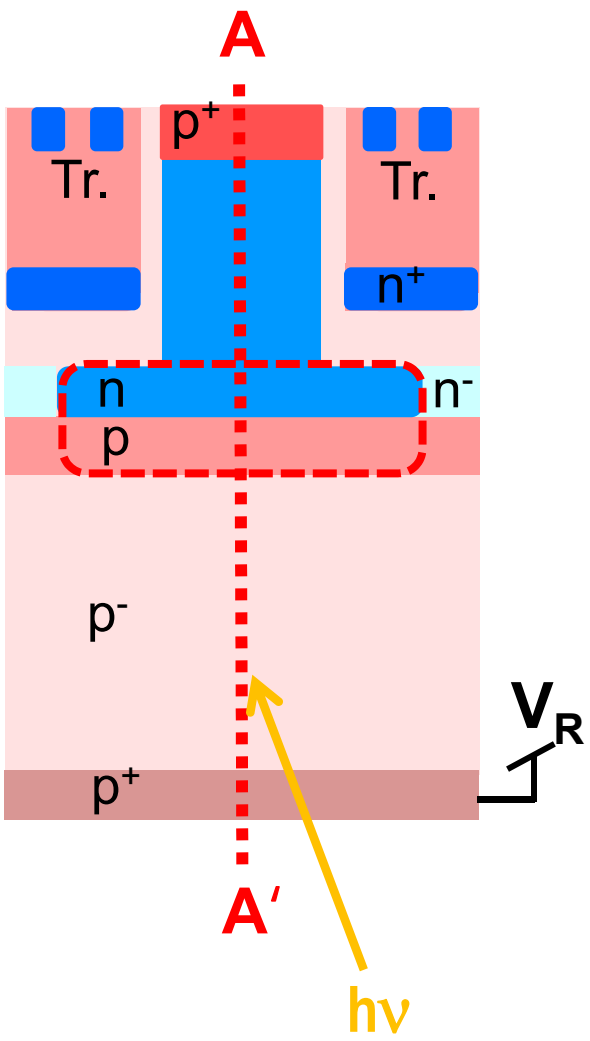
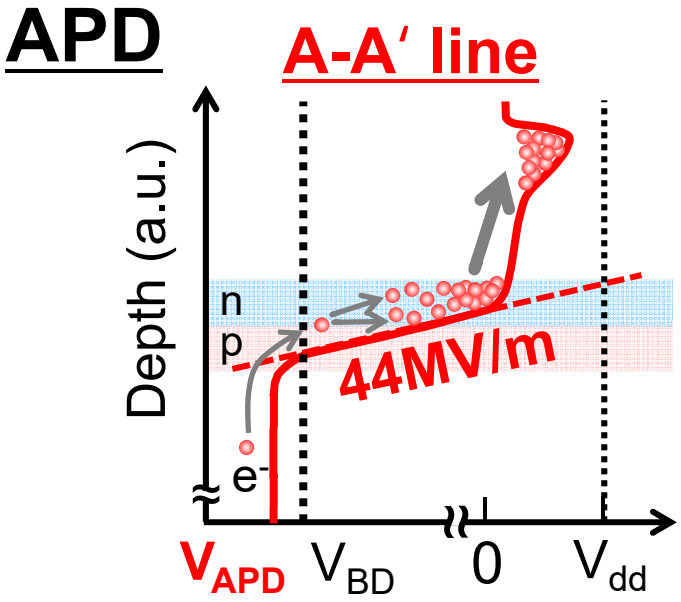
APD Insertion & Isolating Tr.-region





$E_{critical}$ = 42MV/m

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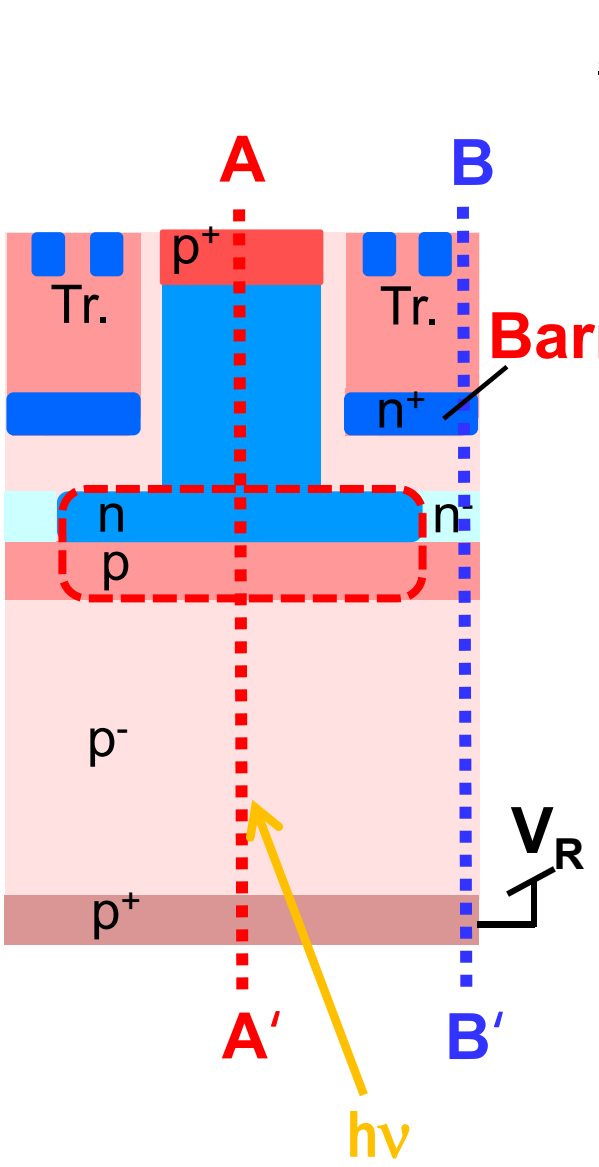
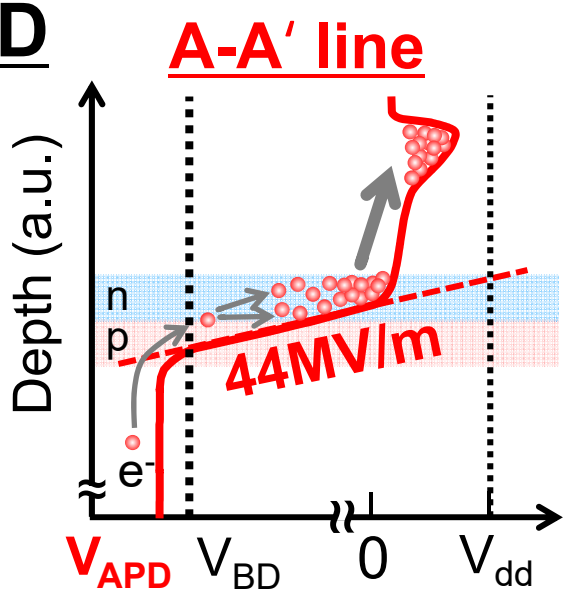
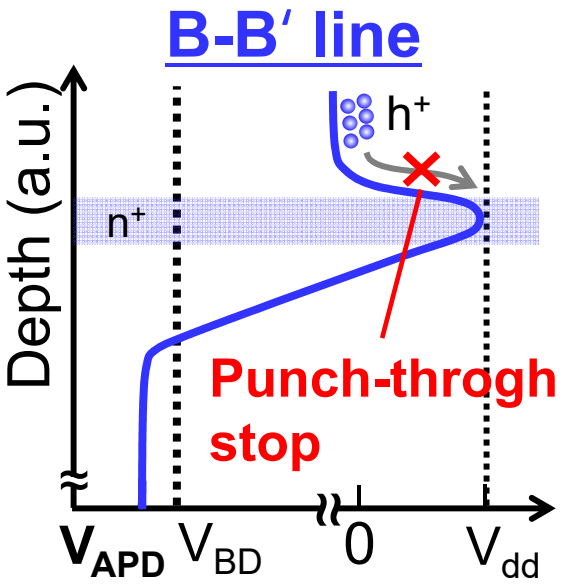
APD Insertion & Isolating Tr.-region







$E_{critical}$ = 42MV/m

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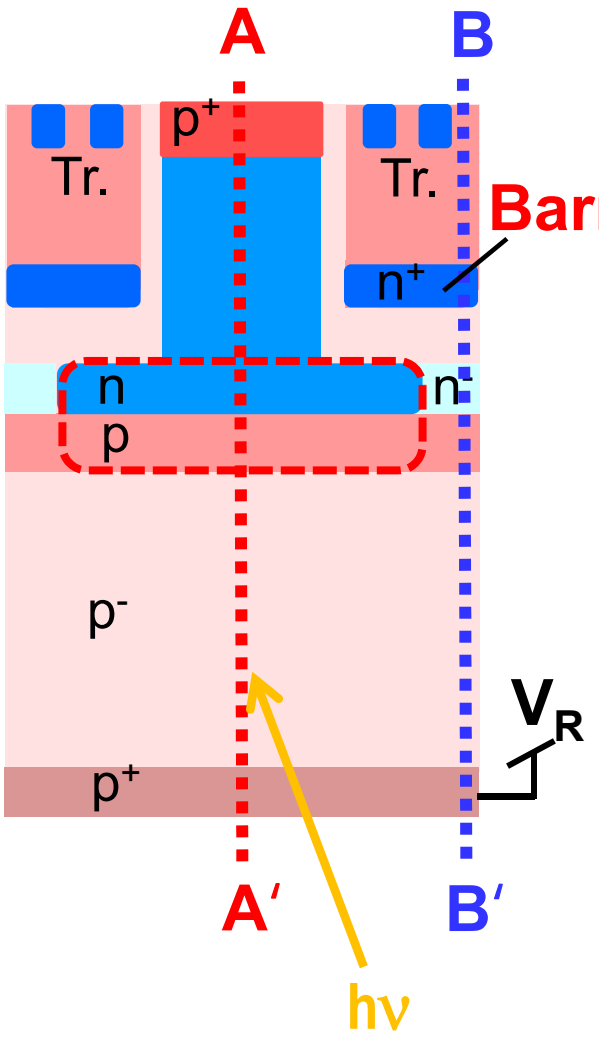
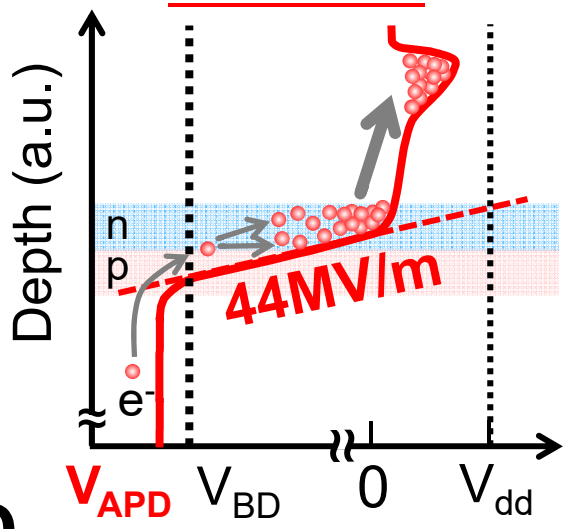
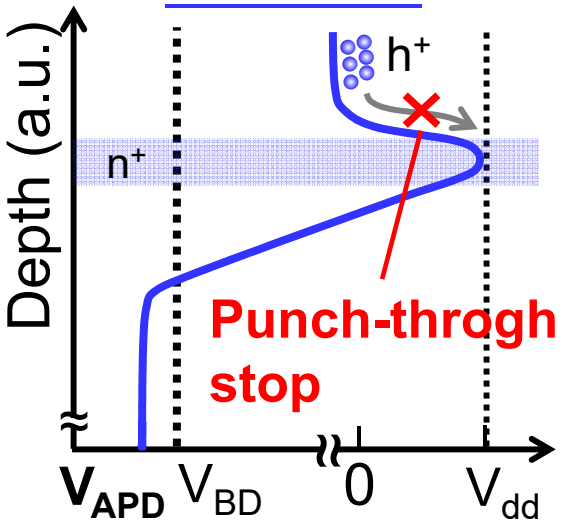
APD Insertion & Isolating Tr.-region

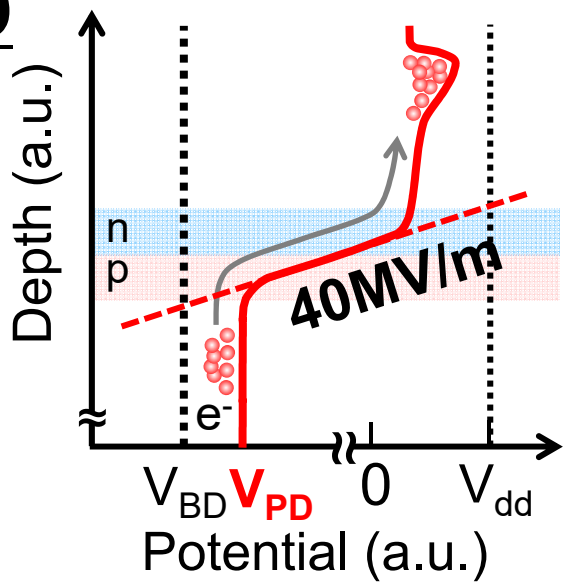


APD





PD



$E_{critical}$ = 42MV/m

V_{PD} tolerance

$|V_{PD}| < |V_{BD}|-3V$

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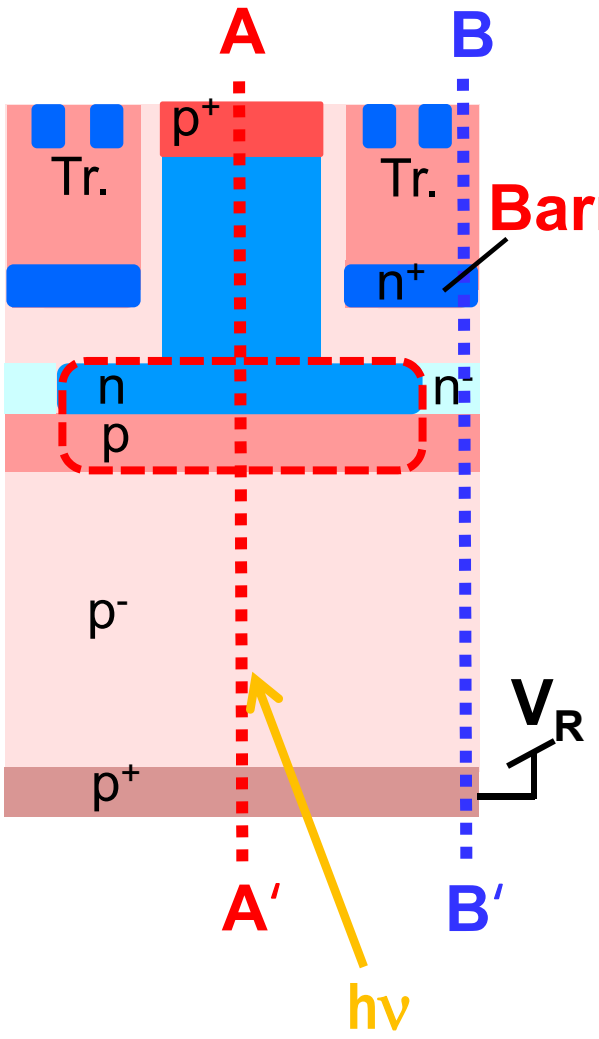
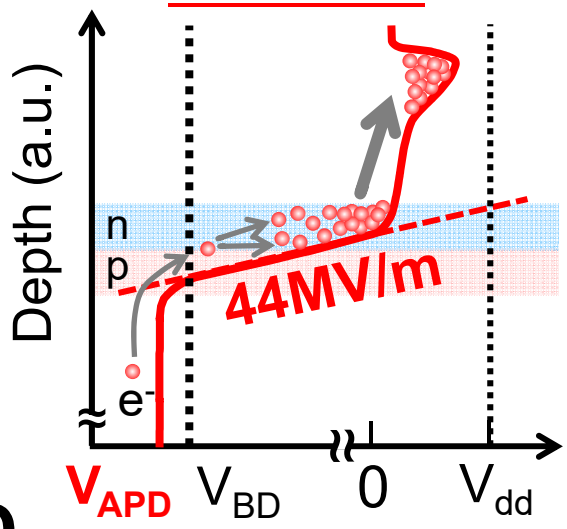
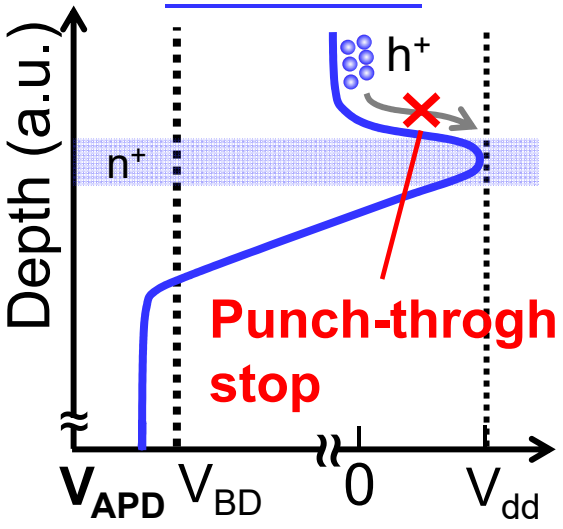
APD Insertion & Isolating Tr.-region

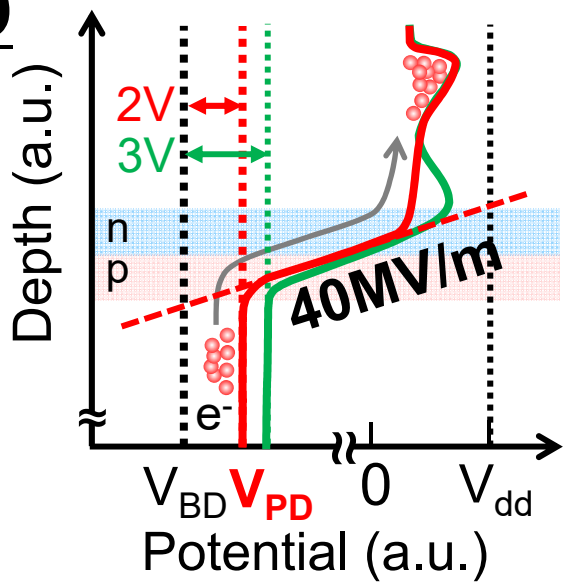


APD





PD



$E_{critical}$ = 42MV/m

V_{PD} tolerance

$|V_{PD}| < |V_{BD}|-3V$

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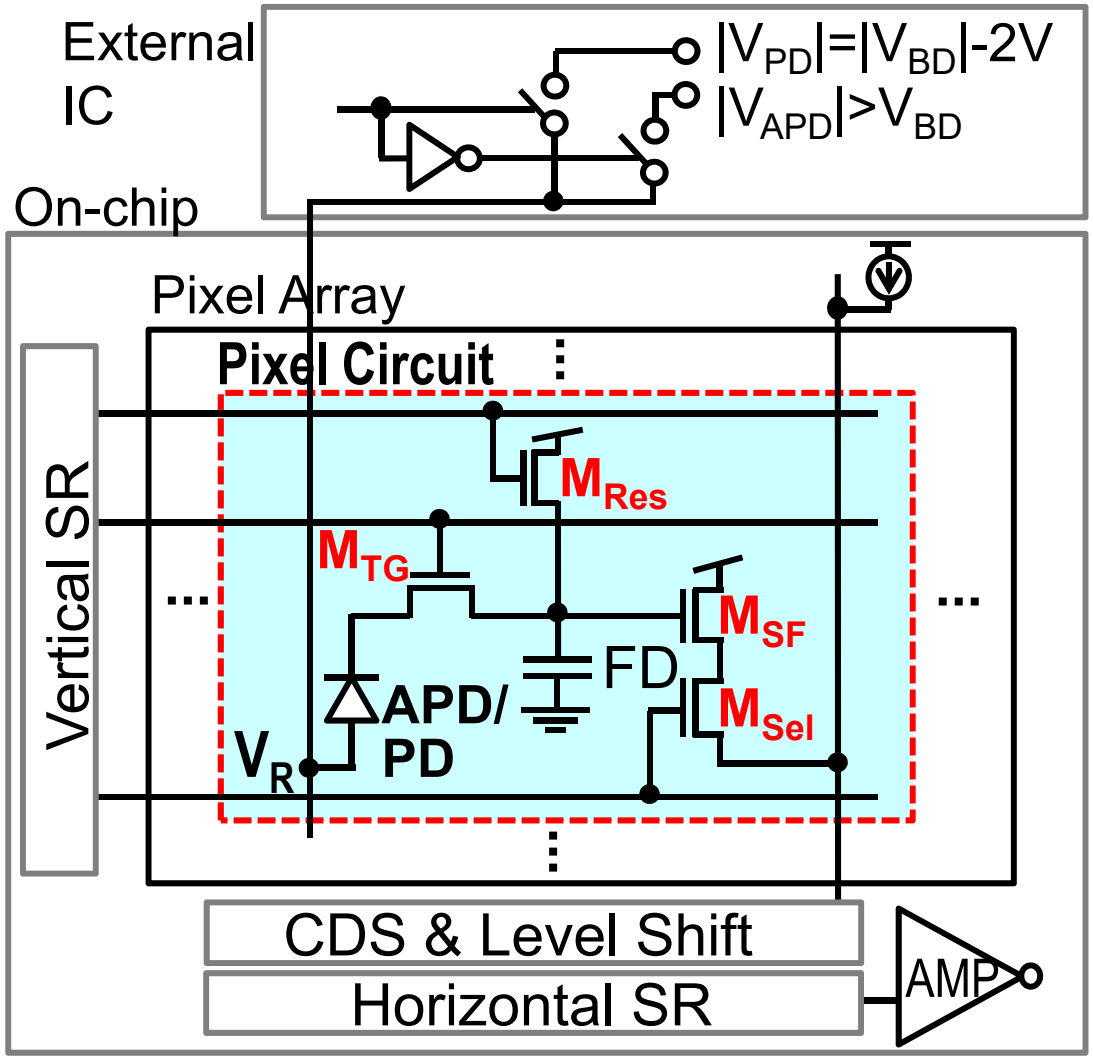
Chip Architecture

4-Tr. configuration + external Voltage IC



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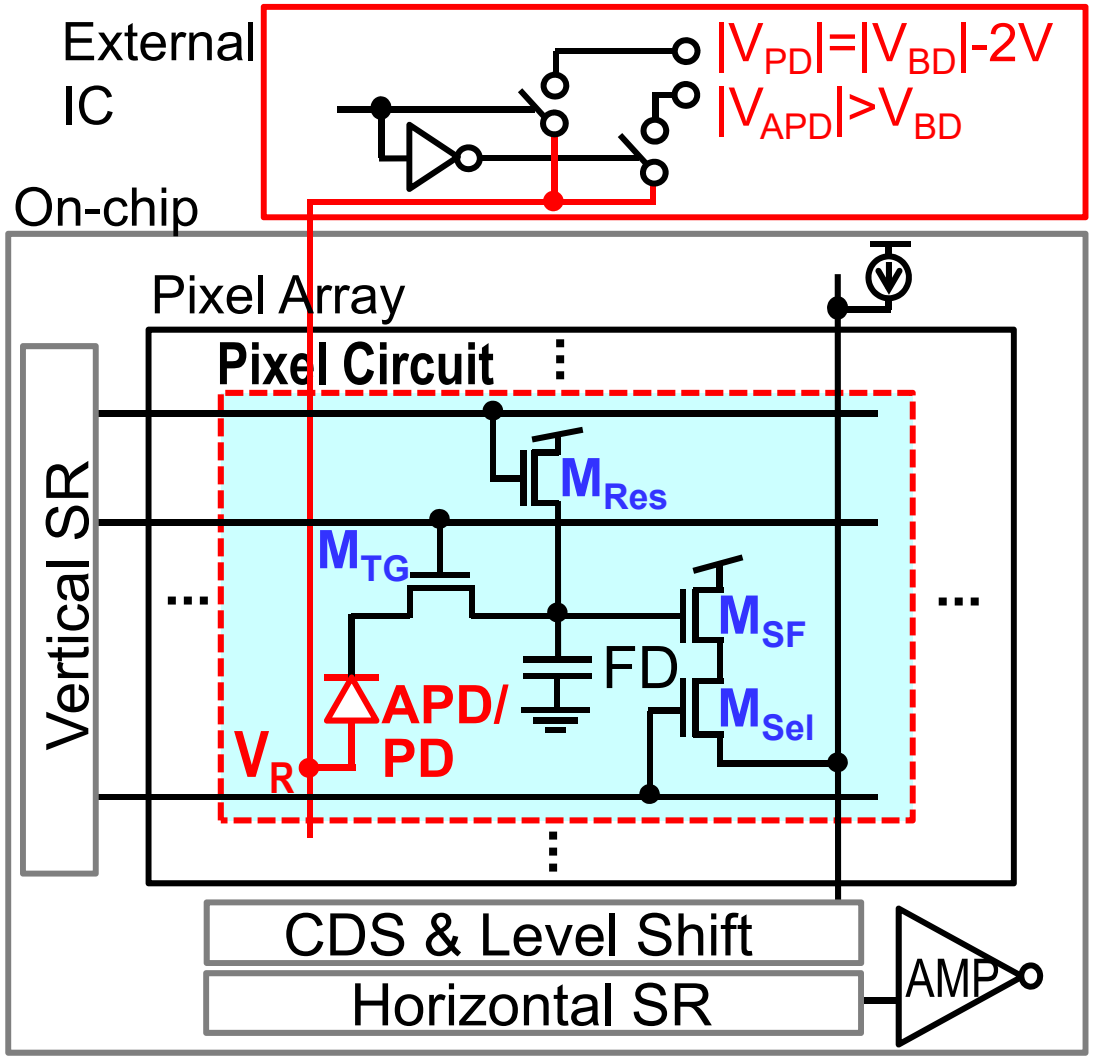
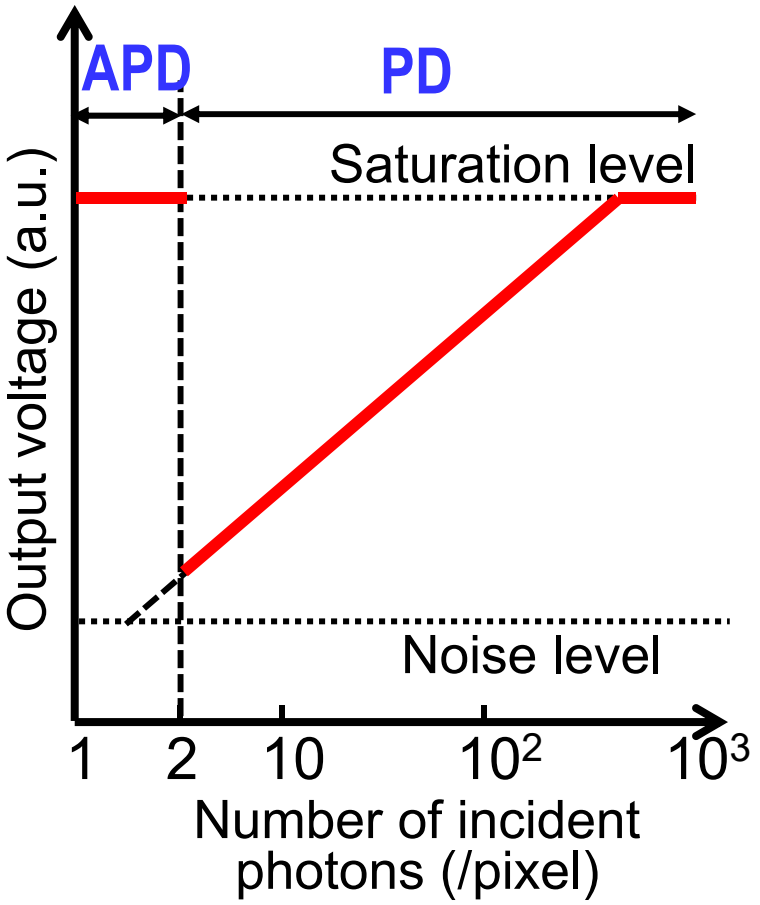
Chip Architecture

4-Tr. configuration + external Voltage IC





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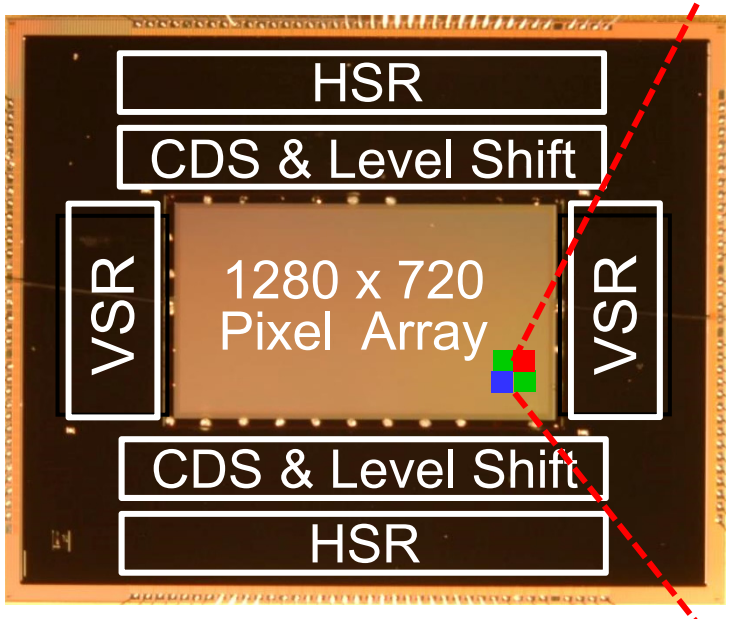
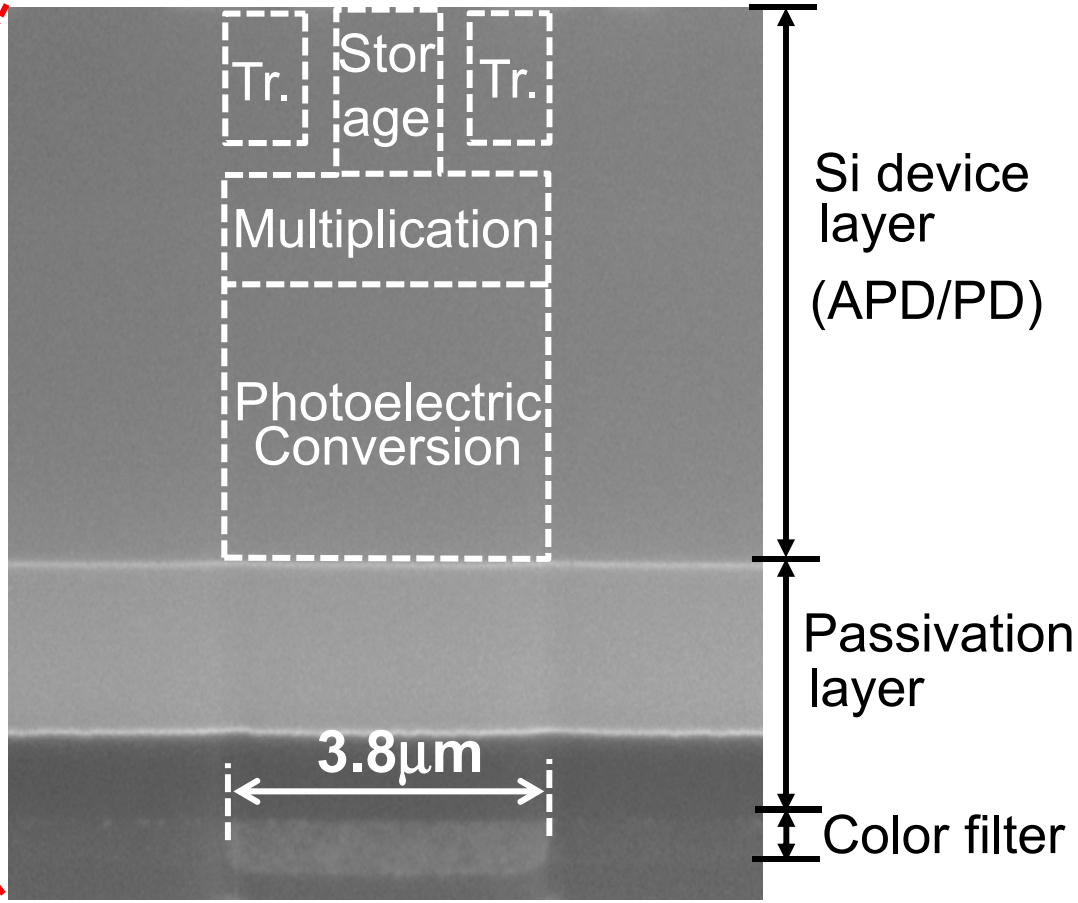
Fabricated Sensor Device

Pixel size: 3.8μm, 110nm CMOS with 1Poly 4Metal

Chip Photo



Cross-sectional SEM image



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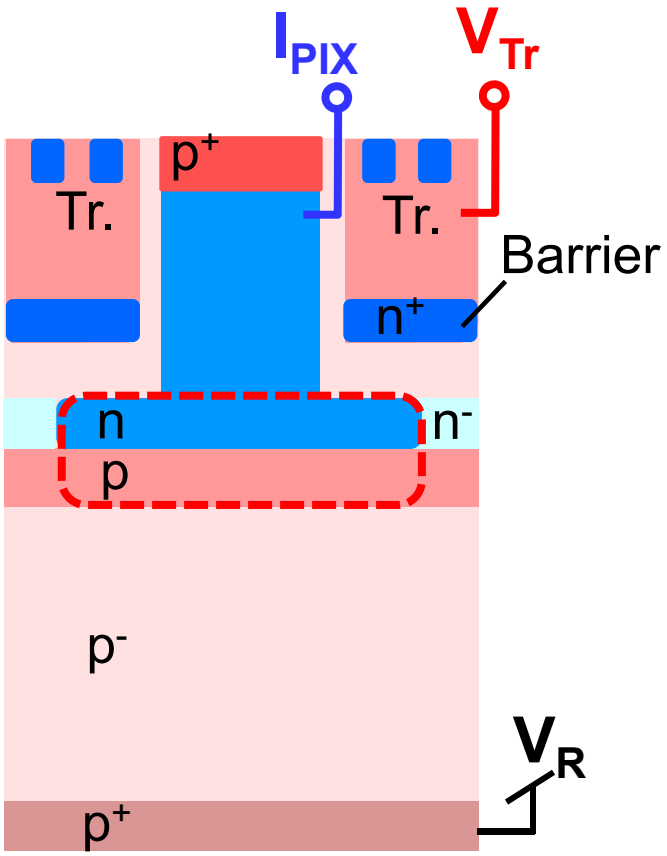
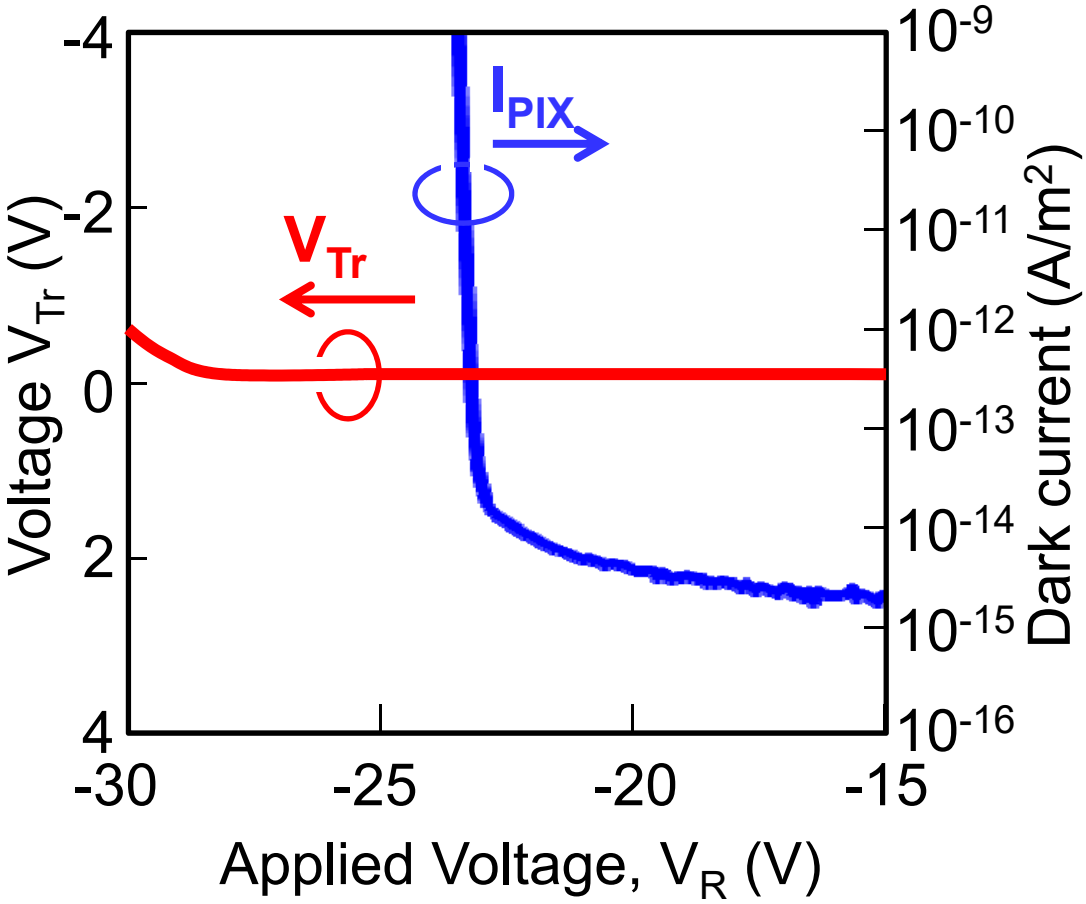
Isolation Characteristics

Prevent punch-through breakdown





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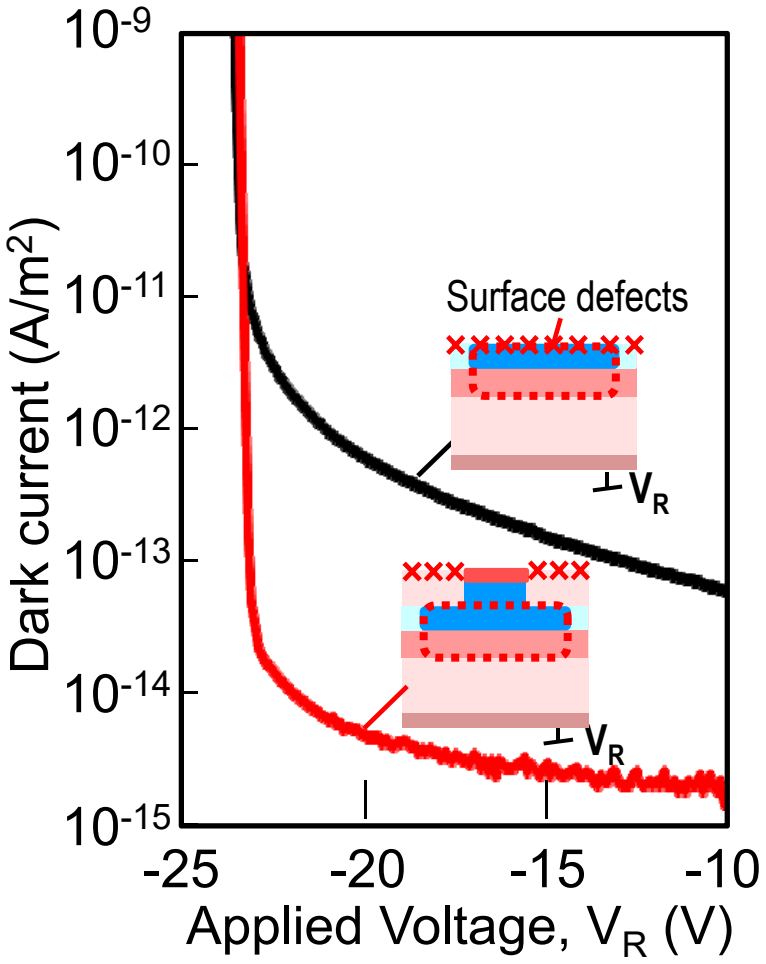
Dark Current, Multiplication, DCR



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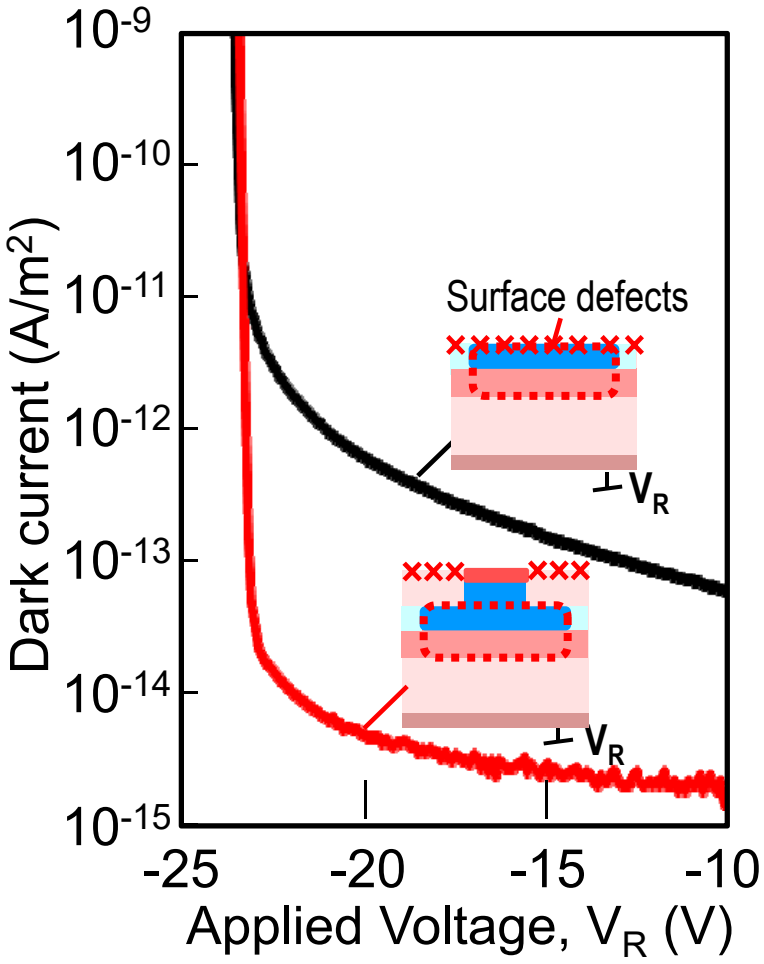
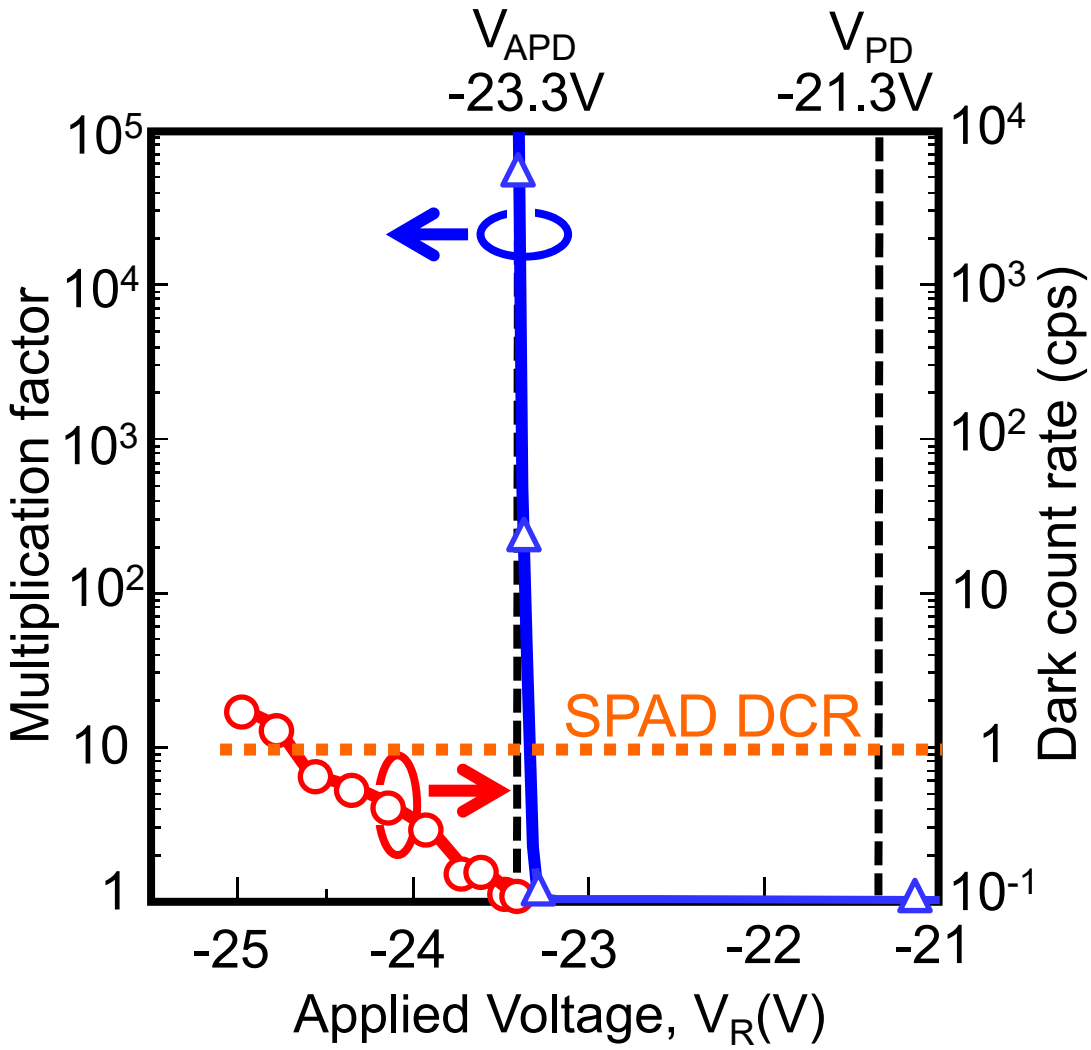
Dark current, Multiplication, DCR

Low DCR 0.1cps at high multiplication factor of 10^5





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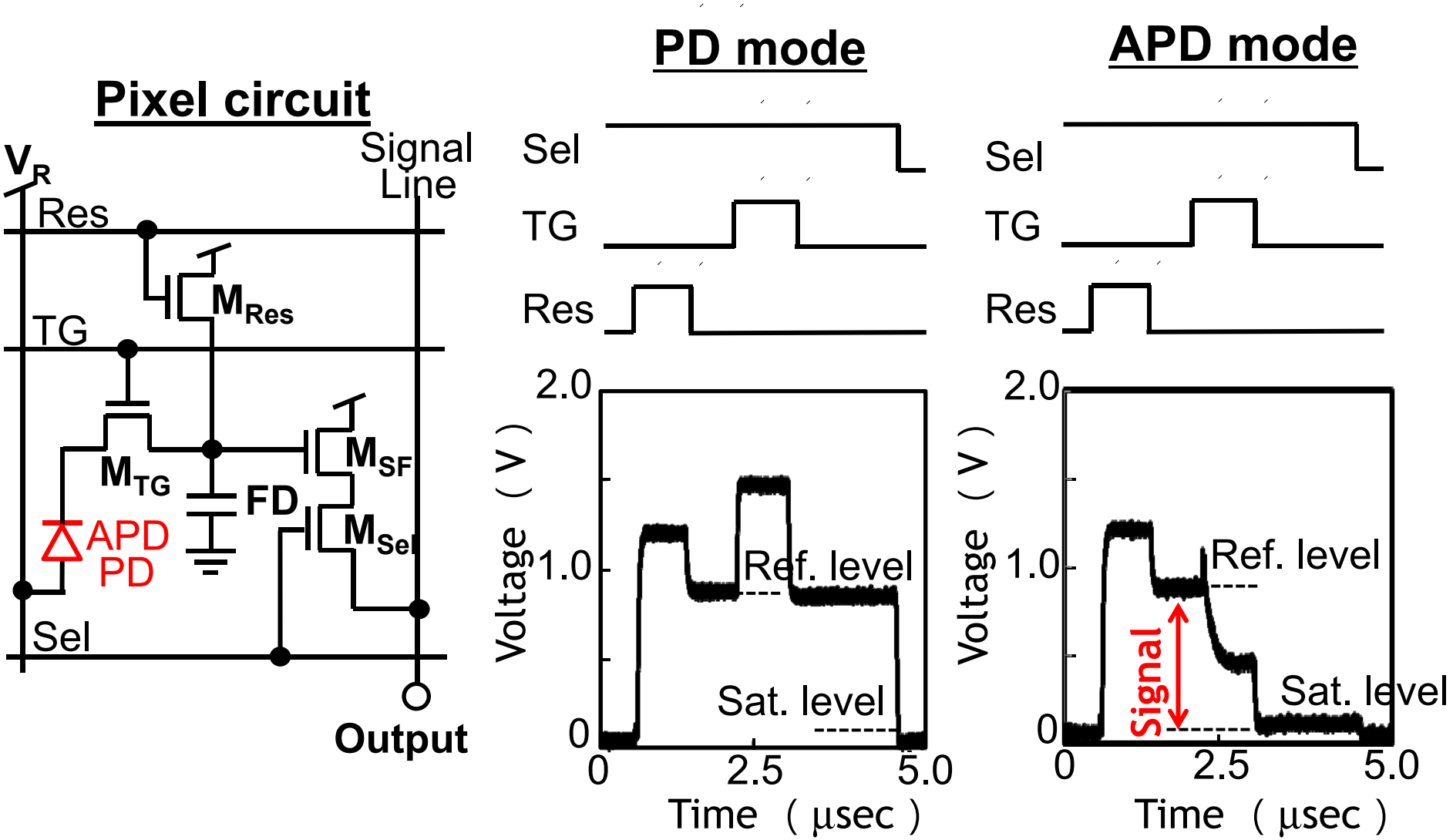
Signal Output at APD/PD Mode

Output of saturation level by high multiplication ratio



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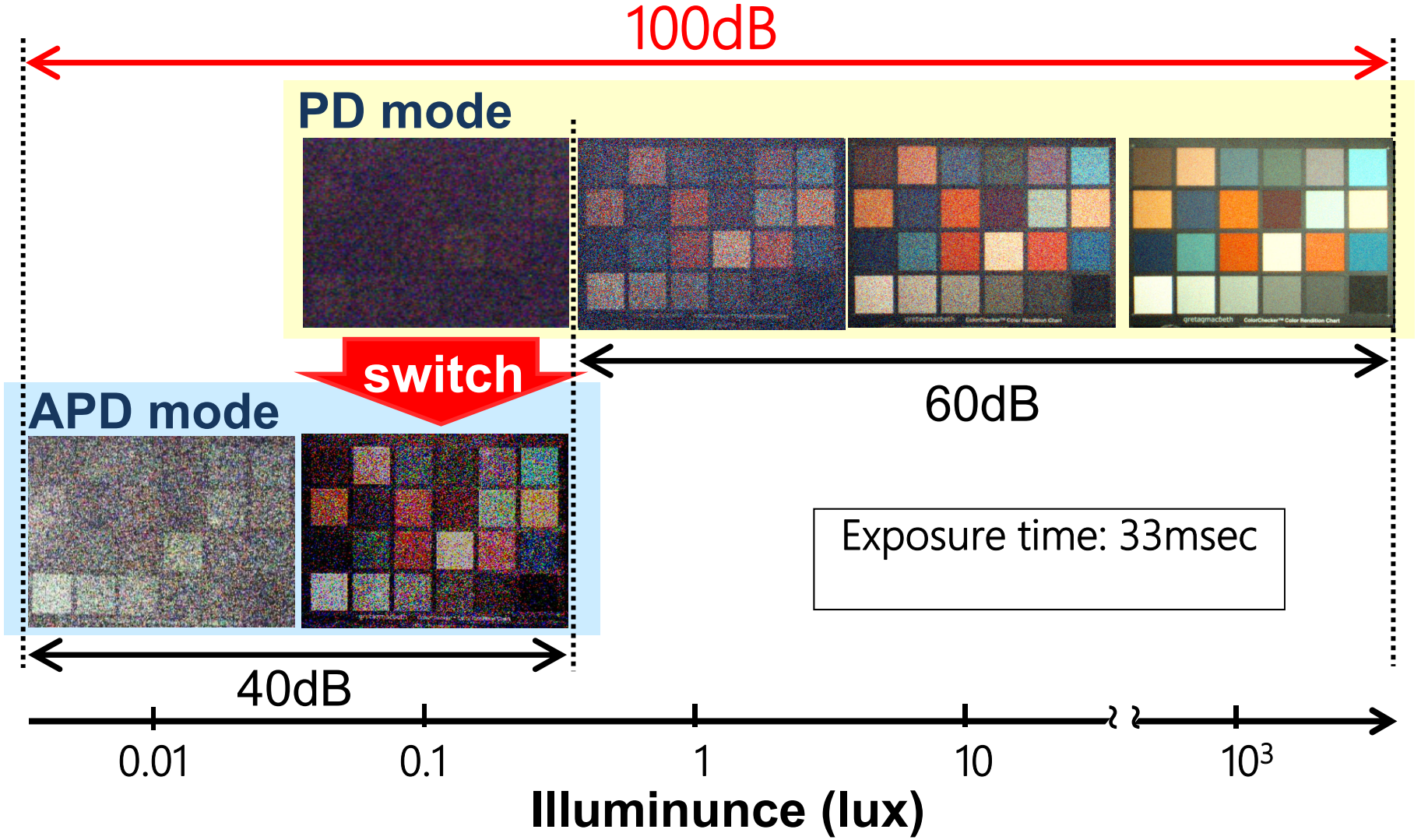
Reproduced Images

Dynamic Range 100dB by switching APD/PD mode



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Summary

An APD/PD switchable CMOS image sensor is realized.

Achievements

- APD natural color imaging: 0.01lux
- Wide dynamic range: 100dB
- Number of pixels: 1280x720 , Pixel-size: 3.8μm

Expected

Real-time imaging in both dark and bright to open up new applications

Surveillance cameras, Car-mounted cameras, ..

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A 1.2e$^-$ Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA

Kei Shiraishi, Yasuhiro Shinozuka, Tomonori Yamashita, Kazuhide Sugiura, Naoto Watanabe, Ryuta Okamoto, Tatsuji Ashitani, Masanori Furuta and Tetsuro Itakura

Toshiba Corporation, Kawasaki, Japan

TOSHIBA
Leading Innovation

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Outline

- Background
- Proposed readout circuits
- Measurement results
- Summary

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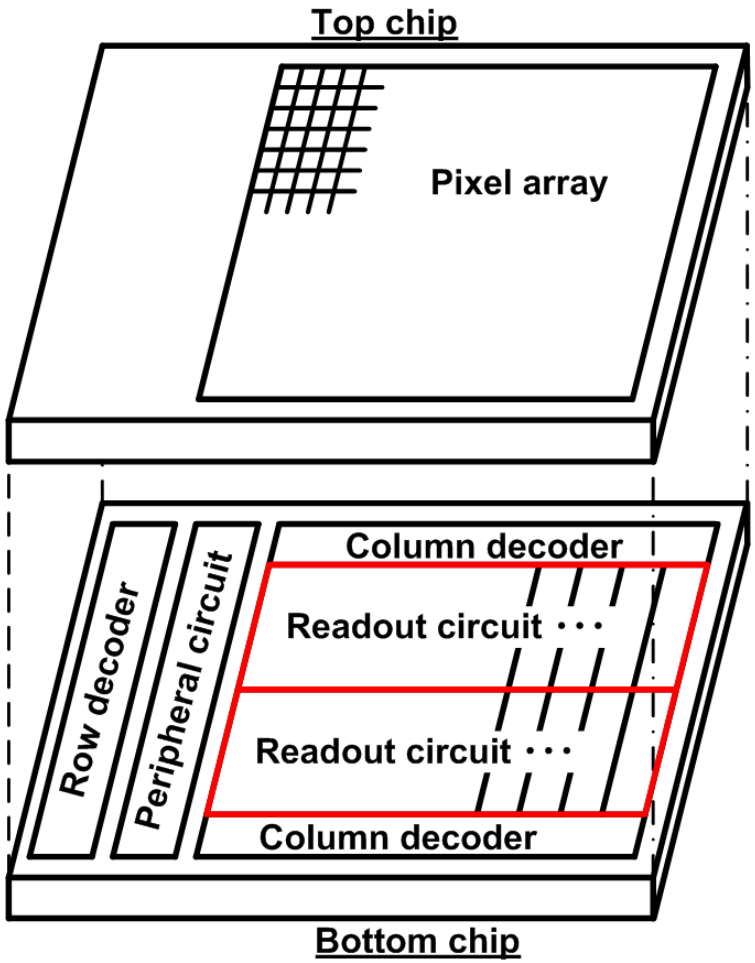
Background

- **Background:**
  - Rapid development of smart phones
- **Target:**
  - Low-noise
  - High power-efficiency
- **Approach:**
  - High performance readout circuits
  - 3D-stacking
    - Larger area for readout
    - Keeping footprint small



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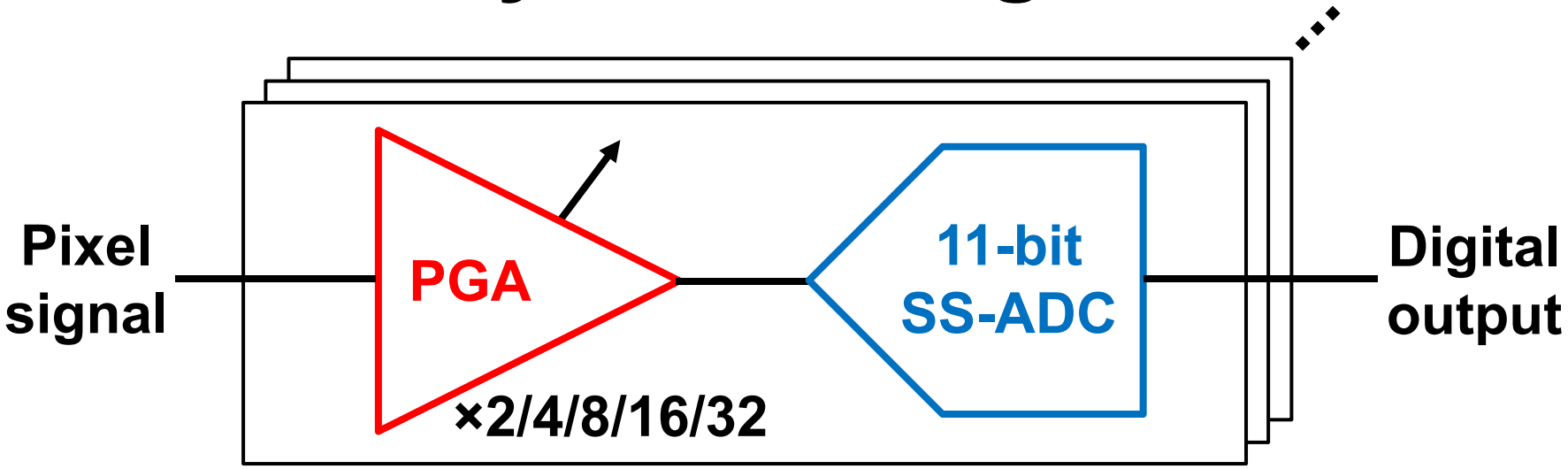
Key Technologies



1. Low-noise and Power-efficient PGA

- Comparator-based switched-capacitor (CBSC)
- Multiple-sampling (MS)

2. Low-power SS-ADC

- Look-ahead (LA) scheme

3. High-speed readout

- Pipelined operation of PGA & ADC

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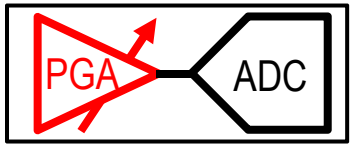
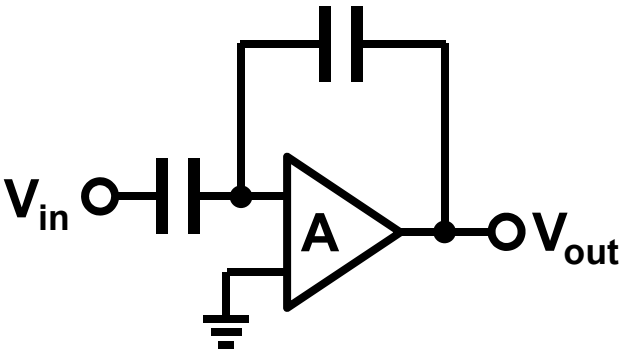
PGA Architecture

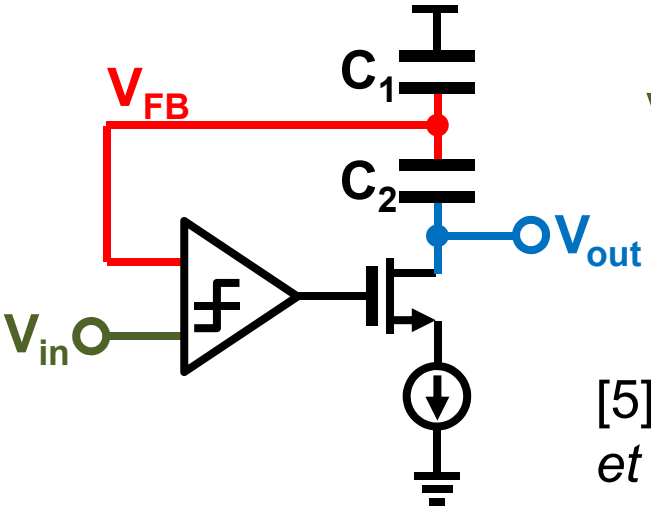


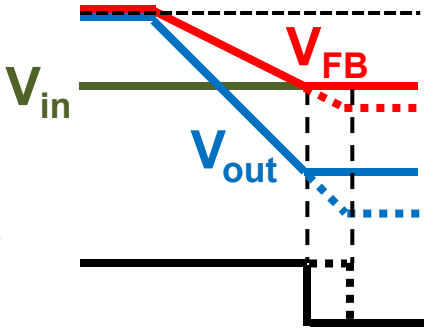
OTA-based PGA



☹ PGA gain sensitive to OTA gain
→Larger power for gain accuracy

Comparator-based PGA





[5] J-K. Fiorenza, *et al*., JSSC 2006

☺ OTA-less architecture
→ Low power

☹ Large offset voltage due to decision delay
→ Cancelled with digital CDS

Comparator-based PGA is suitable for low power CIS

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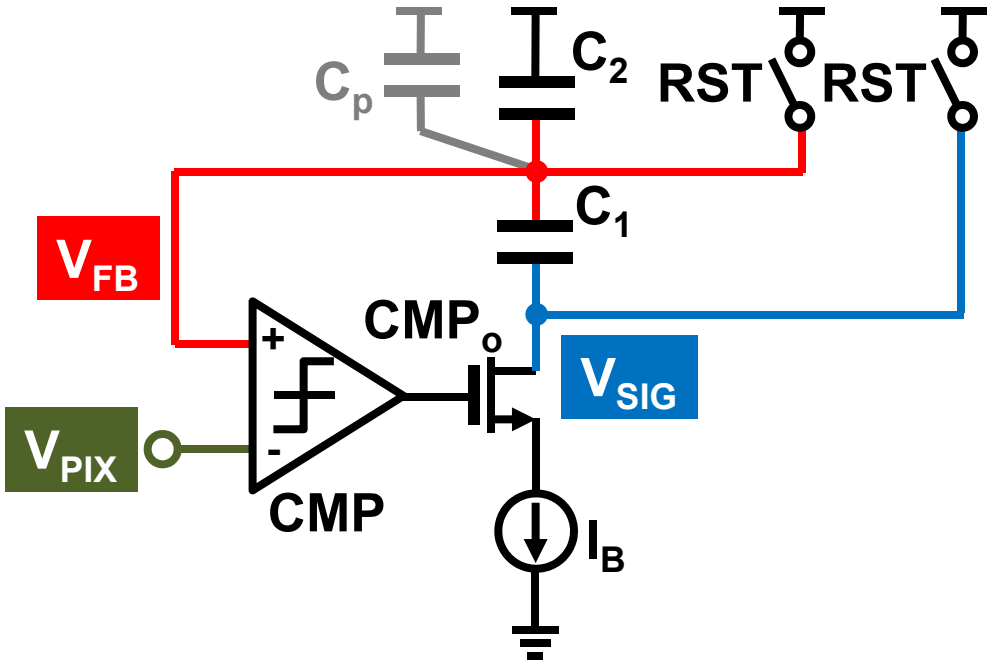
Conv. CBSC-PGA[5]



$$A_{v,conv} = \frac{(C_1 + C_2 + C_p)/I_B}{C_1/I_B}$$

- **PGA gain is sensitive to C_p**
  - PGA gain inaccuracy
  - Variation of C_p → **Column gain mismatch**

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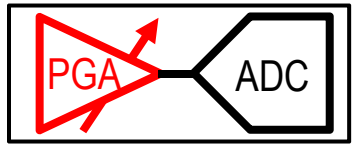
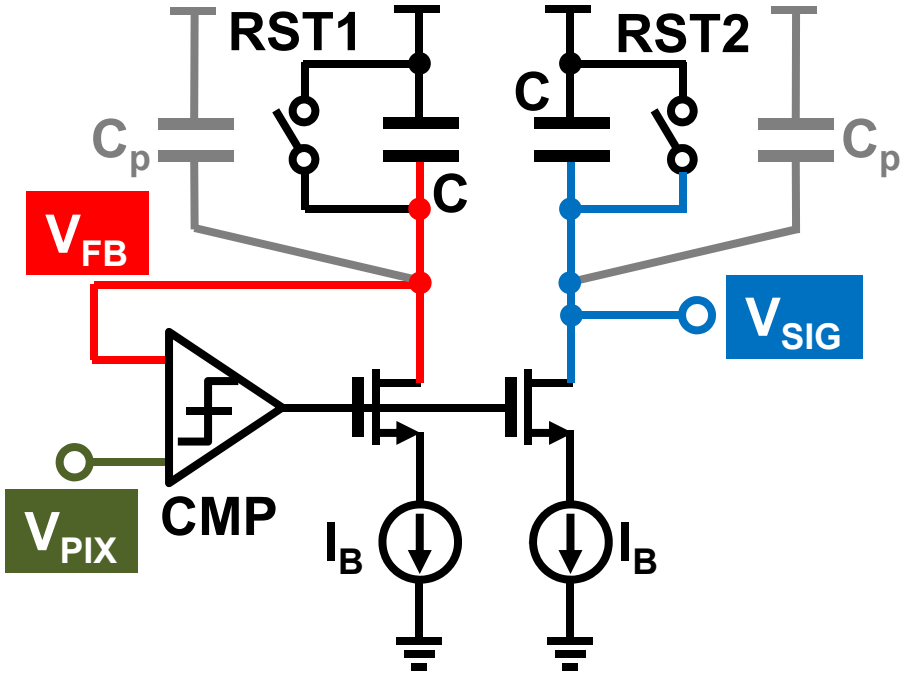
Proposed PGA



Parasitic-insensitive CBSC-PGA



$$A_{v,prop} \approx \frac{(C + C_p)/I_B}{(C + C_p)/I_B} = 1$$

- **Two identical charge pumps**
  - C_p affects 2 charge pumps equally
    - ⇨ **Cancel gain error and mismatch**

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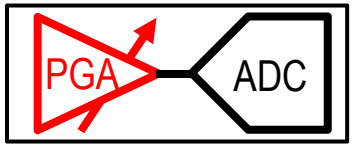
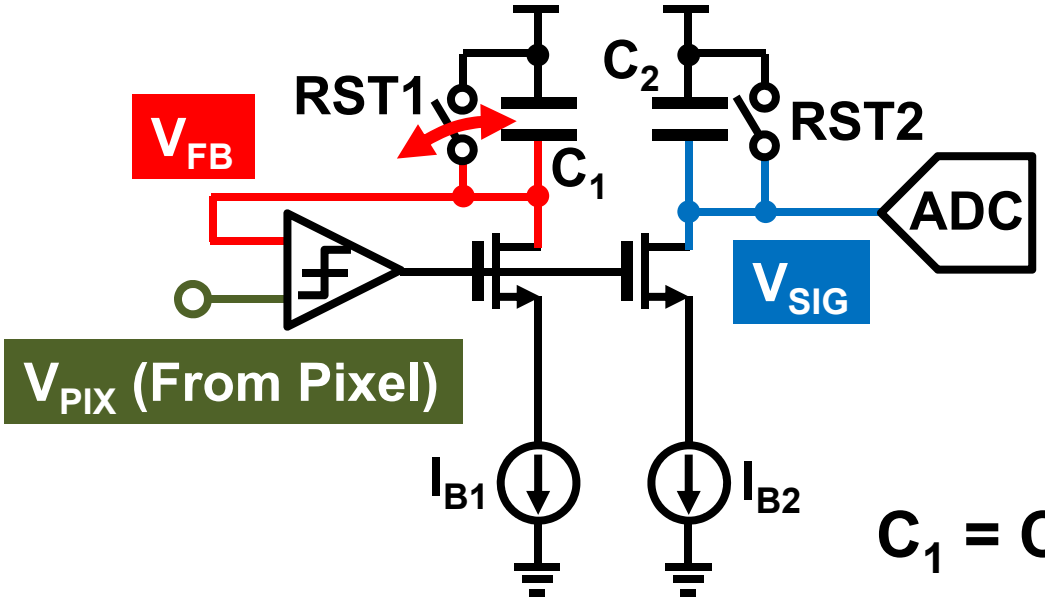
Multiple-Sampling Operation



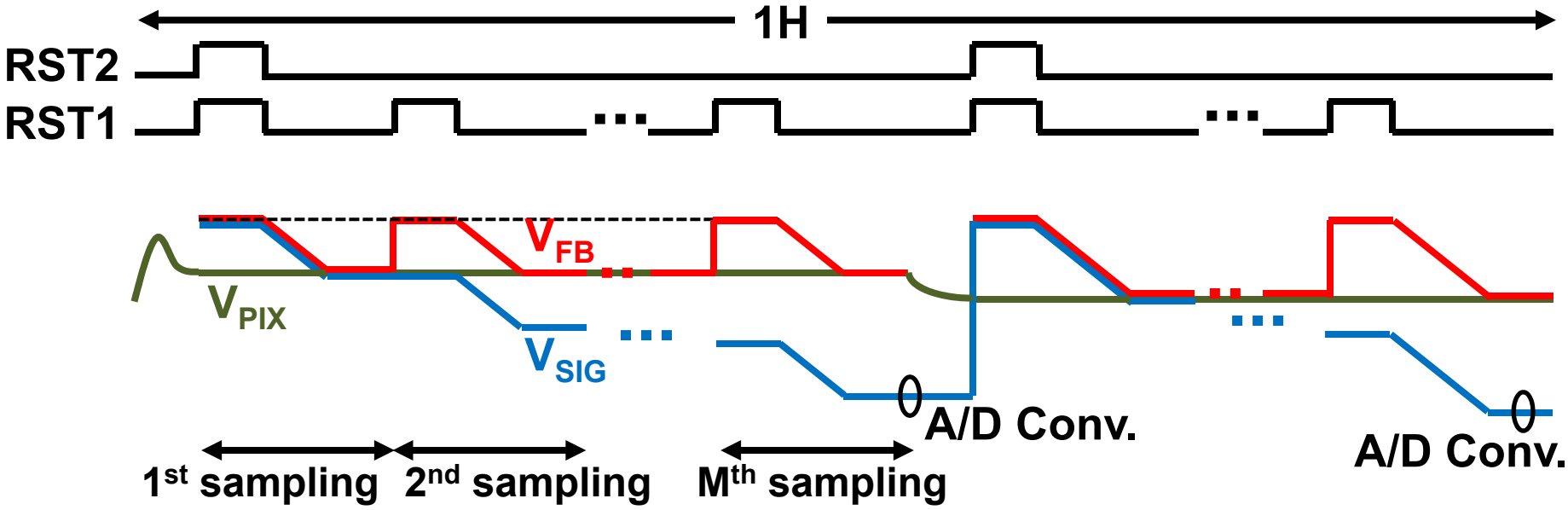


After M times sampling

- Signal: M×
- Noise: $\sqrt{M}$×

→ SNR: $\sqrt{M}$×

$C_1 = C_2$, $I_{B1} = I_{B2}$



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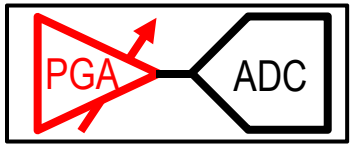
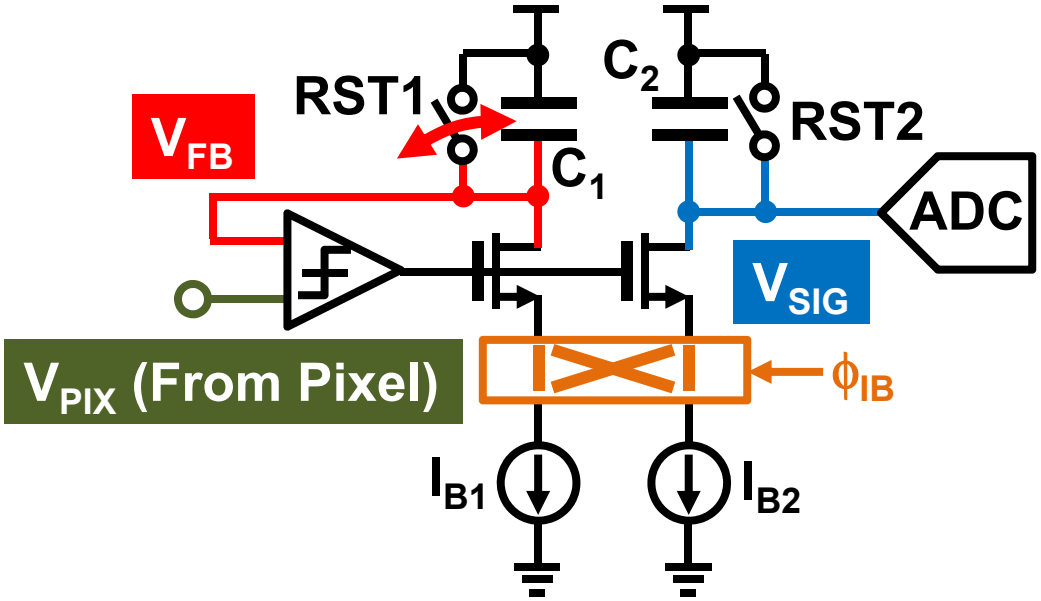
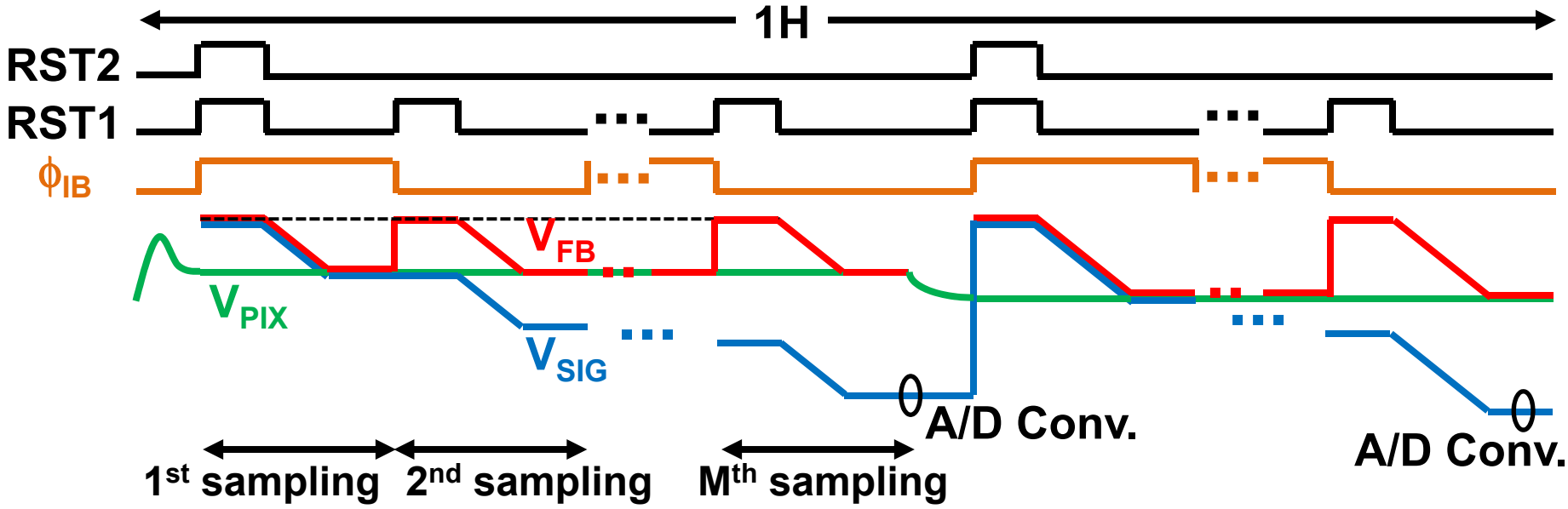
Multiple-Sampling Operation





After M times sampling

- Signal: M×
- Noise: $\sqrt{M}$×
  → SNR: $\sqrt{M}$×
- I_B mismatch cancel



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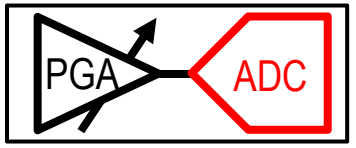
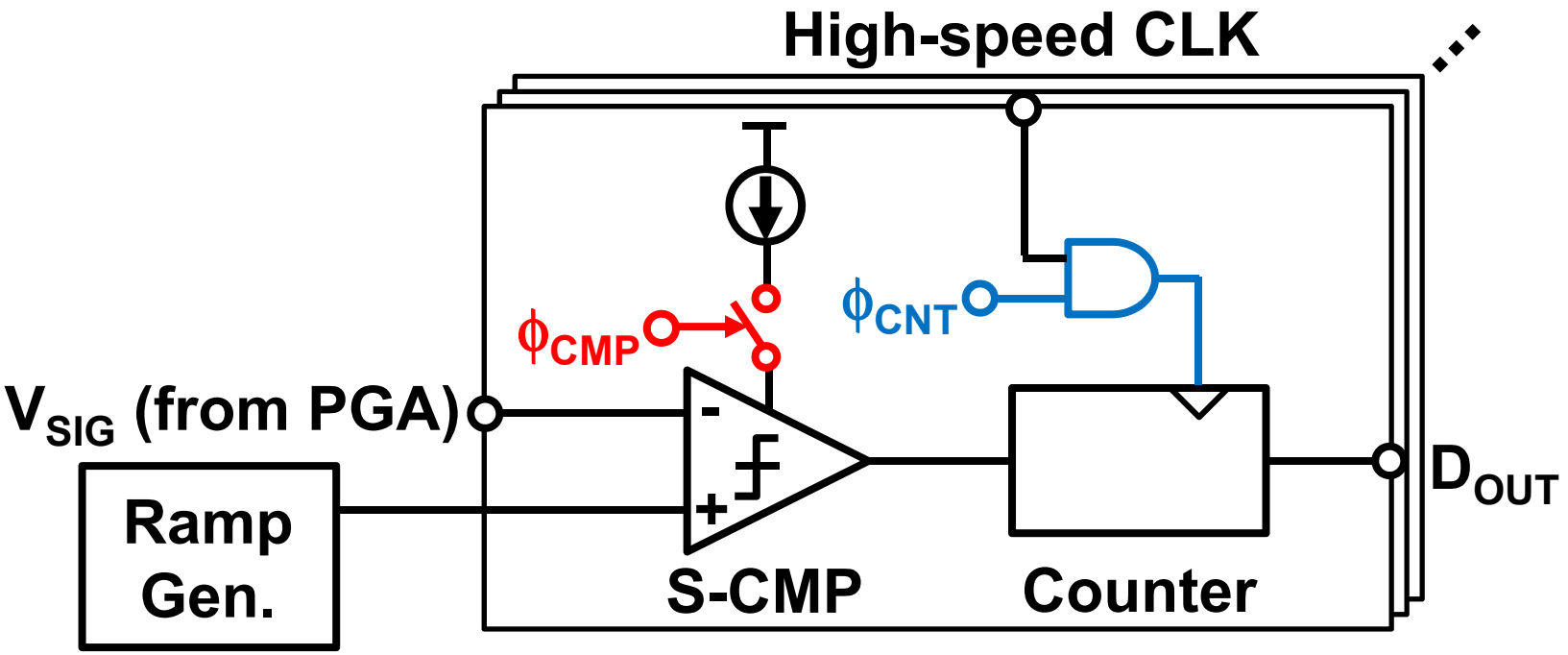
Power/Clock Gated ADC





- **Power-hungry blocks in SS-ADC**
  - S-CMP → **Power-gating**
  - Counter → **CLK-gating**

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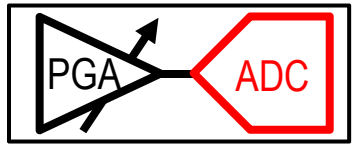
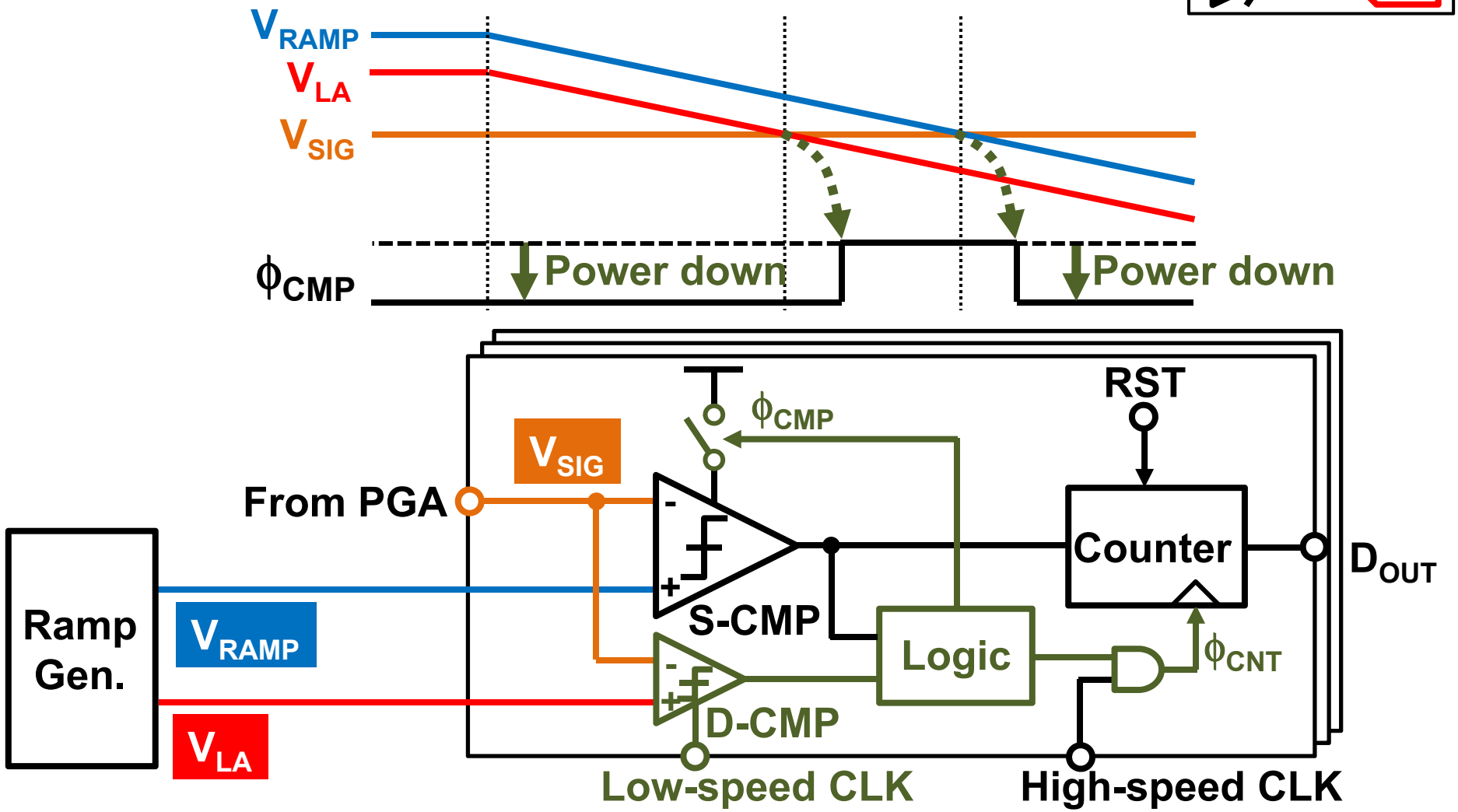
Look-Ahead SS-ADC





- **LA-scheme to predict input signal**

  ⇨ **50% power reduction of column ADC**

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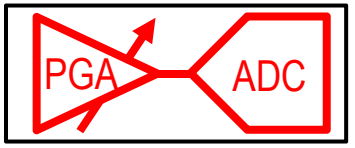
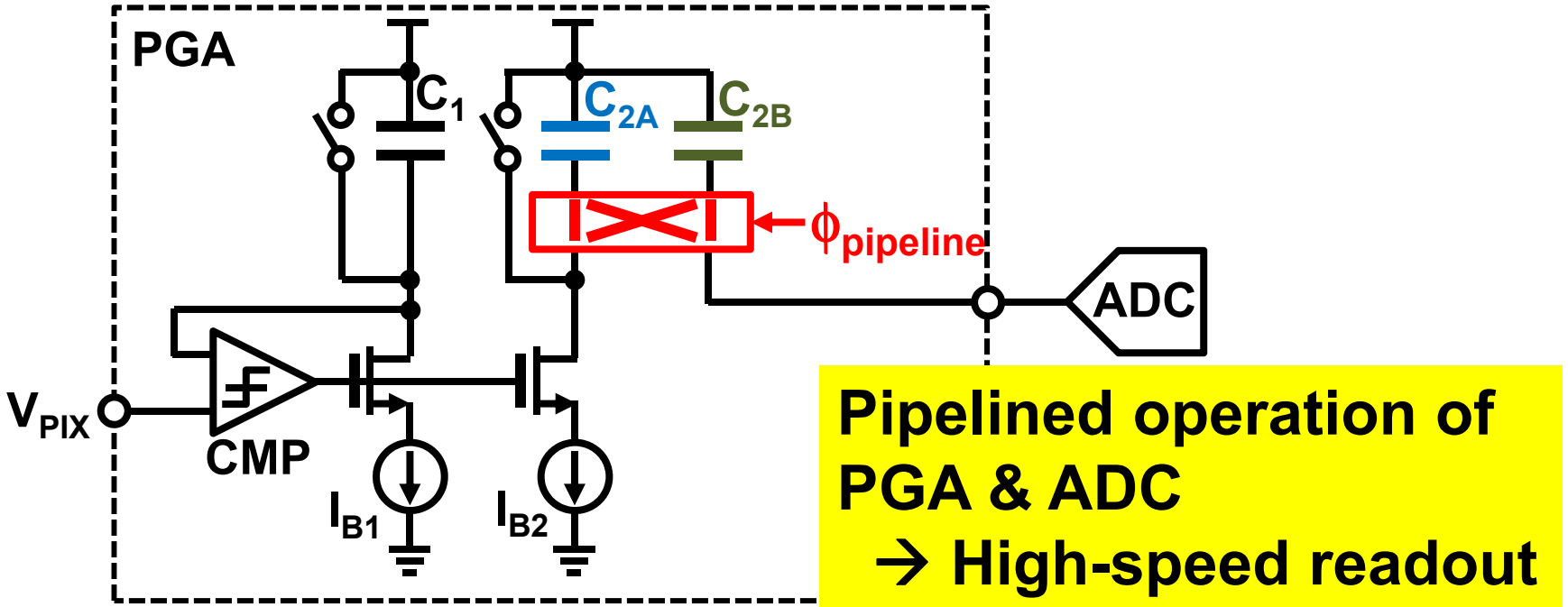
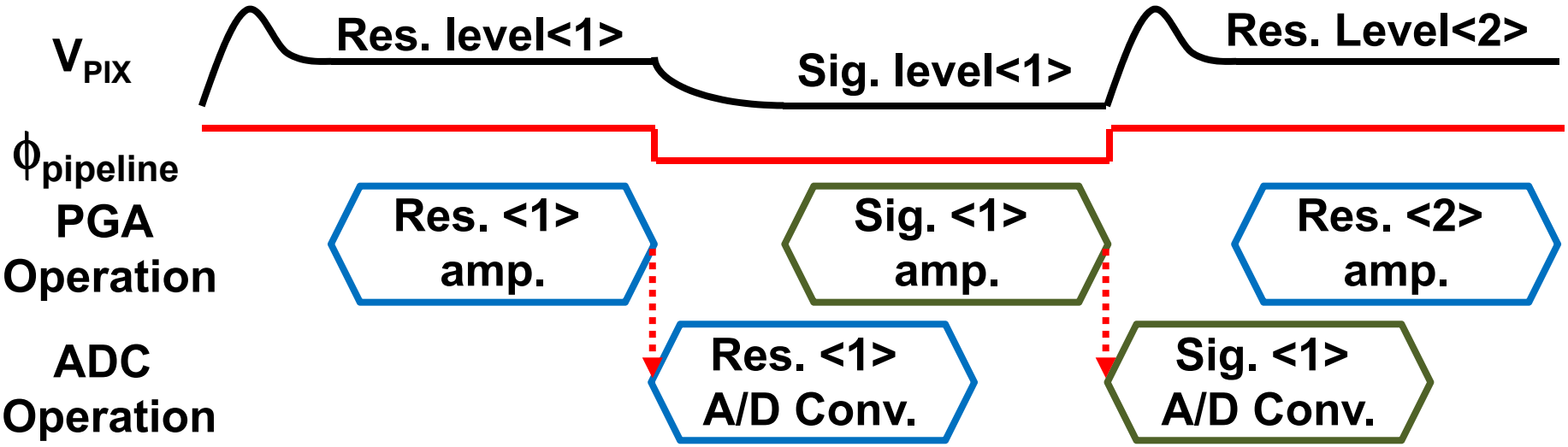
Readout Circuit Operation





Pipelined operation of PGA & ADC
→ High-speed readout



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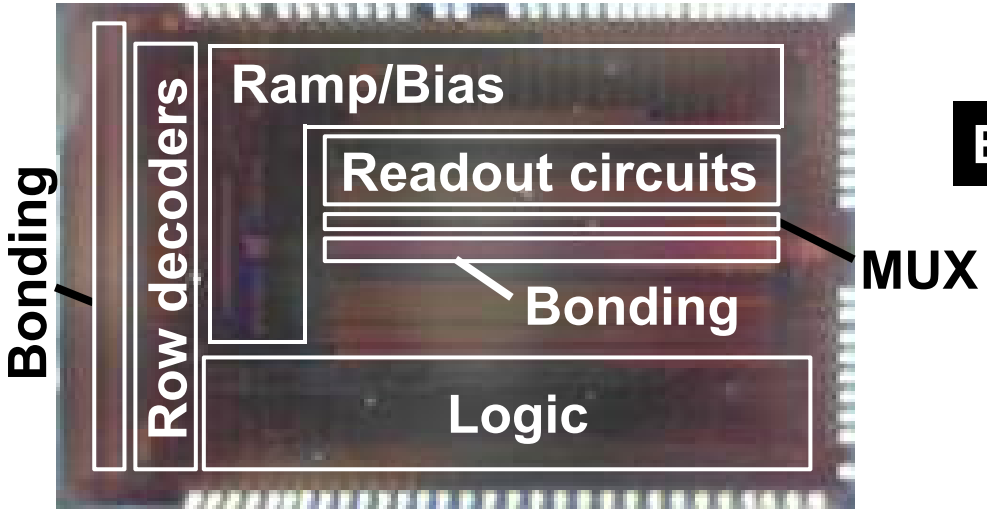
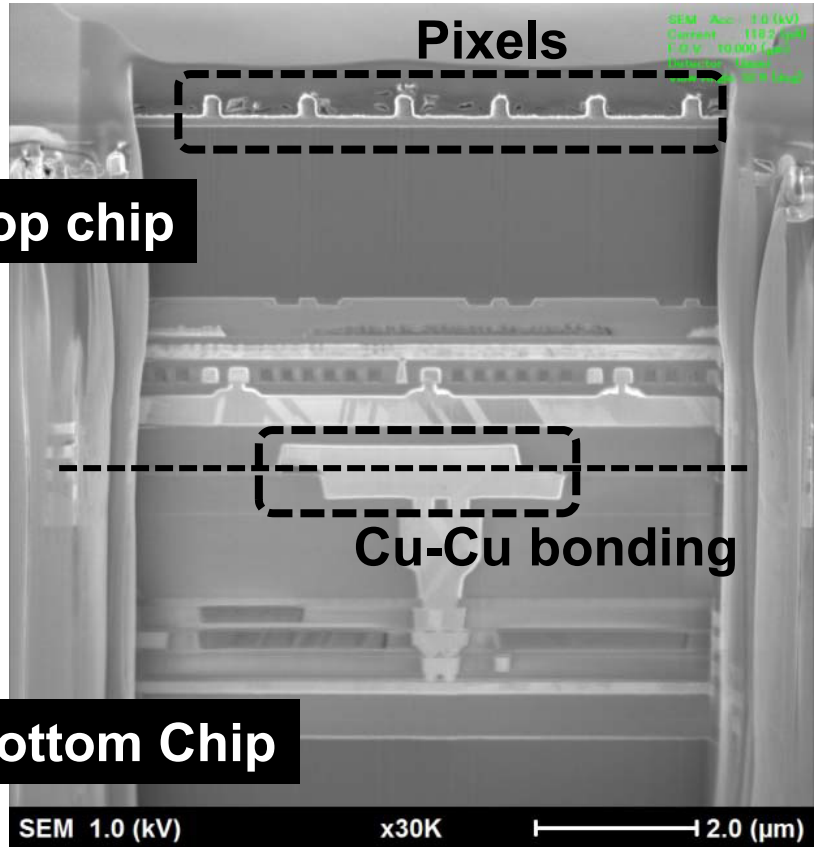
Chip Photos and Cross-Section

Top chip (65nm CIS process)

Bottom chip (65nm CMOS process)



Cross-section



*** 1Mpixel out of full 8Mpixel are selected with analog MUX**

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Sample Image at 16× Sampling

* 8 frames are synthesized to obtain 8Mpixel image

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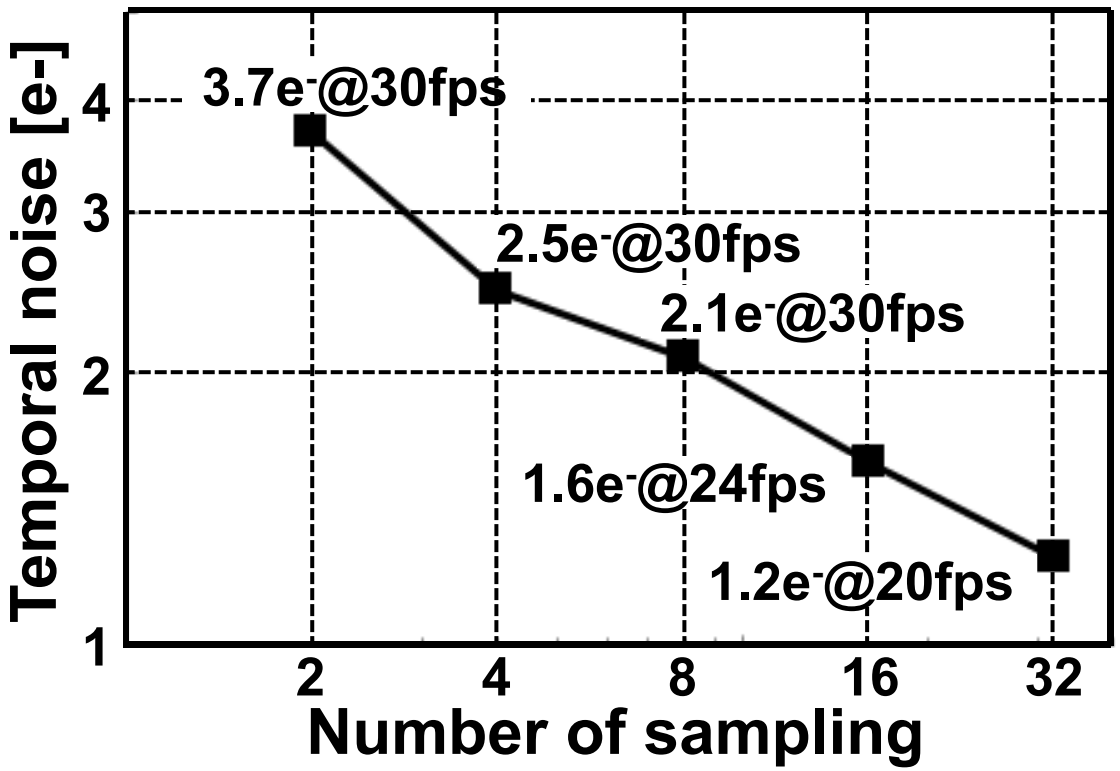
Measured Temporal Noise



* Measured with 1Mpixel

- **Temporal noise**
  - Effectively reduced by # sampling
- **1.2e- with high frame rate (20fps)**

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Performance Summary

Process	Top Chip	65nm CIS	
	Bottom Chip	65nm CMOS	
Supply voltage	Analog	2.5V	
	PLL/IO	1.8V	
	Digital	1.2V	
# of pixels	Full resolution	8M	
	1-frame	1M	
Pixel pitch		1.12um	
Number of sampling		16	32
Total power [mW]		81	104
Frame rate [fps]		24	20
Temporal noise [e-]		1.6	1.2

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Summary

- A 3D-stacked CMOS image sensor for mobile application

- Multiple-sampling technique
  → 1.2e$^-$ temporal noise @32× sampling
- An SS-ADC with look-ahead scheme
  → 50% power reduction of column ADC
- Pipelined operation of PGA and ADC
  → 20fps @32× sampling

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Thank you for your attention.

We have the demonstration session today in the Golden Gate Hall.

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References

[1] Y. Chae, *et al.*, "A 2.1Mpixel 120frame/s CMOS Image Sensor with Column-Parallel ΔΣ ADC Architecture," *ISSCC Dig. Tech. Papers*, pp. 394-395, Feb. 2010.

[2] J-H. Kim, *et al.*, "A 14b Extended Counting ADC Implemented in a 24MPixel APS-C CMOS Image Sensor," *ISSCC Dig. Tech. Papers*, pp. 390-391, Feb. 2010.

[3] M-W. Seo, *et al.*, "A Low-Noise High Intrascene Dynamic Range CMOS Image Sensor With a 13 to 19b Variable-Resolution Column-Parallel Folding-Integration/Cyclic ADC", *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 272-283, Jan. 2012.

[4] A. Suzuki, *et al.*, "A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb. 2015.

[5] J. K. Fiorenza, *et al.*, "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658-2668, Dec. 2006.

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A 1.5V 33Mpixel 3D-Stacked CMOS Image Sensor with Negative Substrate Bias

Charles Chih-Min Liu, Manoj M. Mhala, Chin-Hao Chang, Honyih Tu, Po-Sheng Chou, Calvin Chao, Fu-Lung Hsueh

TSMC, Hsinchu, Taiwan

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Outline

- **Motivation**
  - 3D-Stacking & Computational Imaging
- **3D-Connection under Pixel Array**
  - Stitching by unit & Negative Pixel Substrate Bias
- **Digital-Oriented CIS Architecture**
  - Low Power, Noise, Pin Count, & Supply Voltage
- **Circuit Blocks & Features**
- **Performance Summary & Conclusions**

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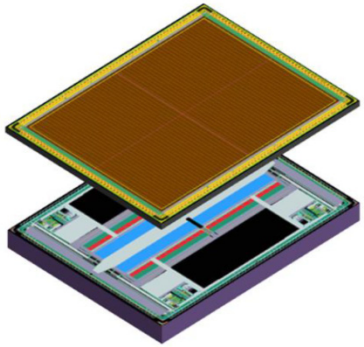
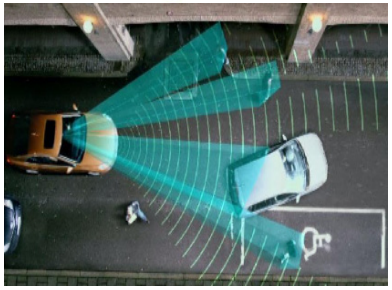
Motivation



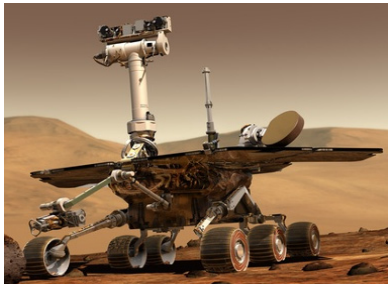
3D stacking separates pixel array and peripheral circuits:



Q: How to fully utilize 3D stacking advantages ?

Q: How to integrate sensor readout circuit with digital image processor to achieve much powerful applications ?

(Target on Advanced CMOS Technology inc. FinFET for fast computation and portable low power)



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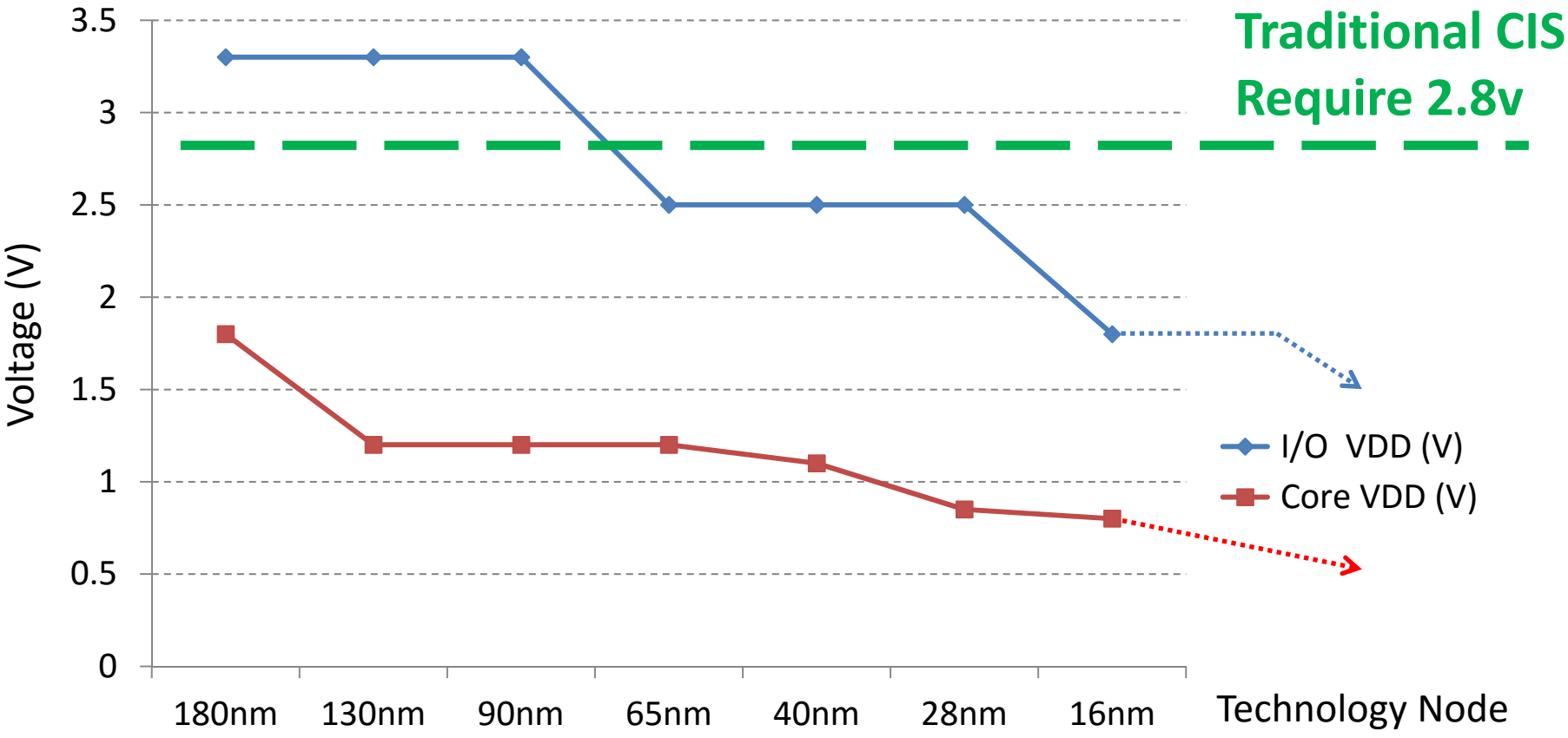
I/O & Core Device Voltage Trend



Technology Node	180nm	130nm	90nm	65nm	40nm	28nm	16nm
I/O VDD (V)	3.3	3.3	3.3	2.5	2.5	2.5	1.8
Core VDD (V)	1.8	1.2	1.2	1.2	1.1	0.85	0.8

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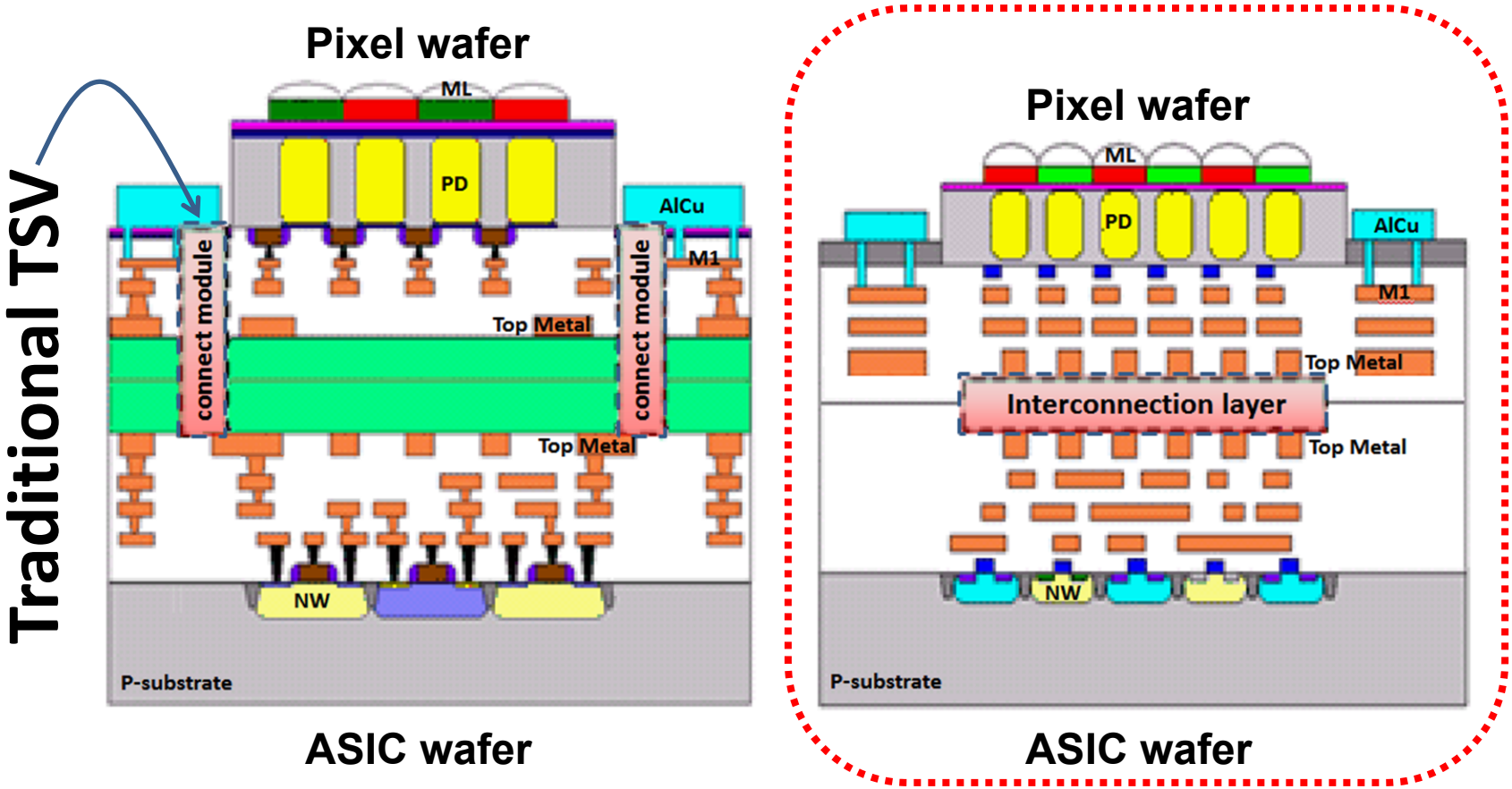
3D-Connection under Pixel Array (Right side)



Common Advantage: Separate Pixel & Circuits development

Special Advantages: Save the TSV through hole area

Realize seamless pixel array stitching

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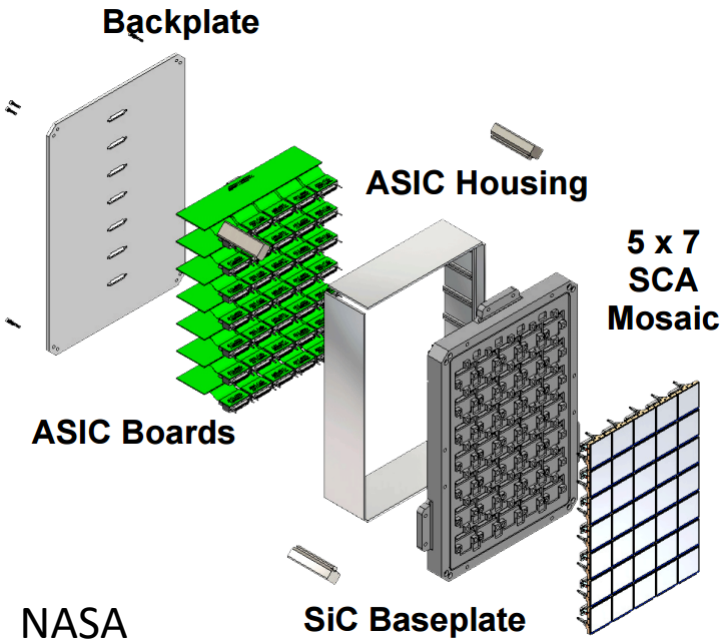
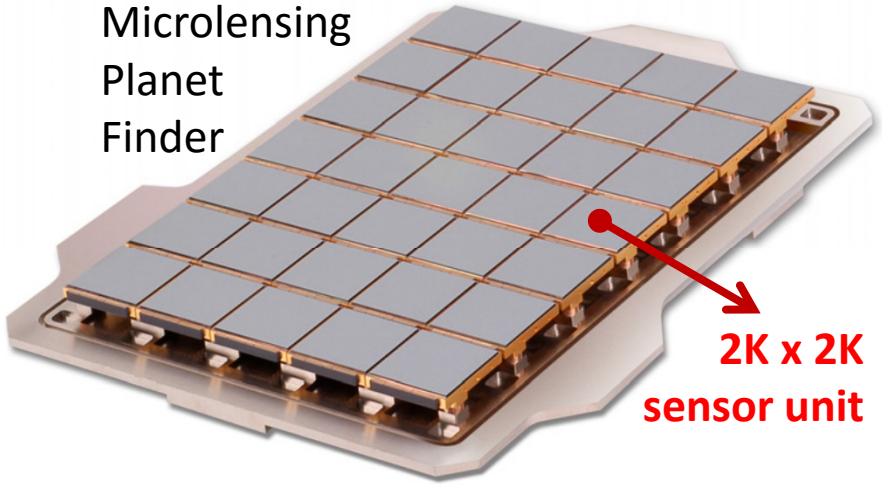
Combined Display units and Sensor units



System level stitched display and sensor have gaps between units.

3D-connection under pixel array is key technology to be seamless.

NASA Microlensing Planet Finder



http://wfirst.gsfc.nasa.gov/science/astro2010_rfi/Astro2010_MPF_RFI.pdf

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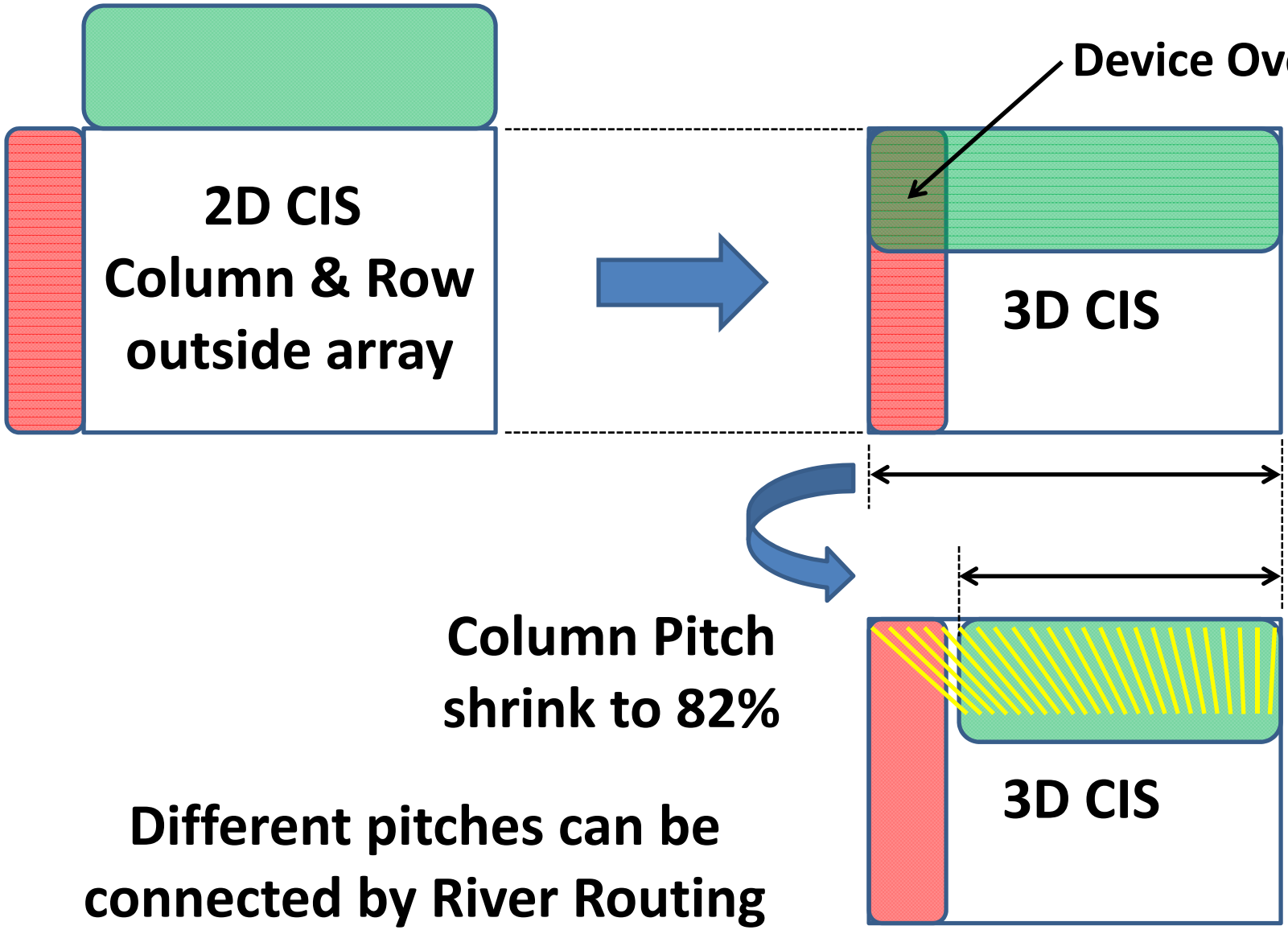
All circuits under Pixel Array



Different pitches can be connected by River Routing

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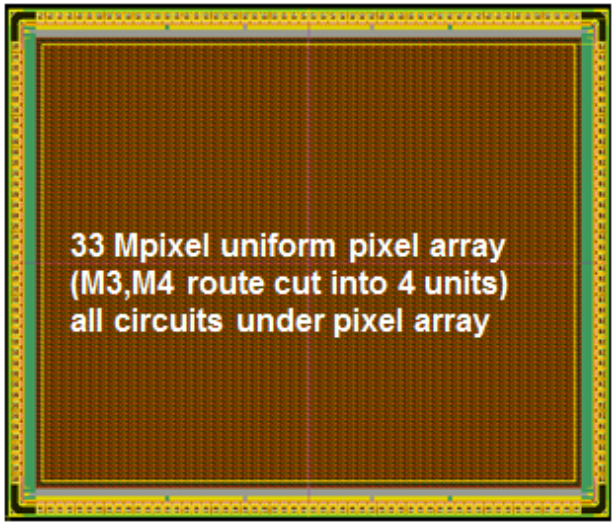
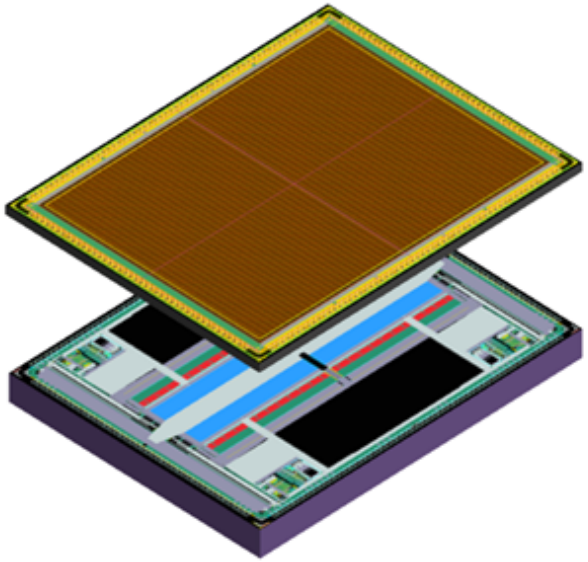
33mp Seamless Readout by 8.3mp units



1P4M PIXEL wafer

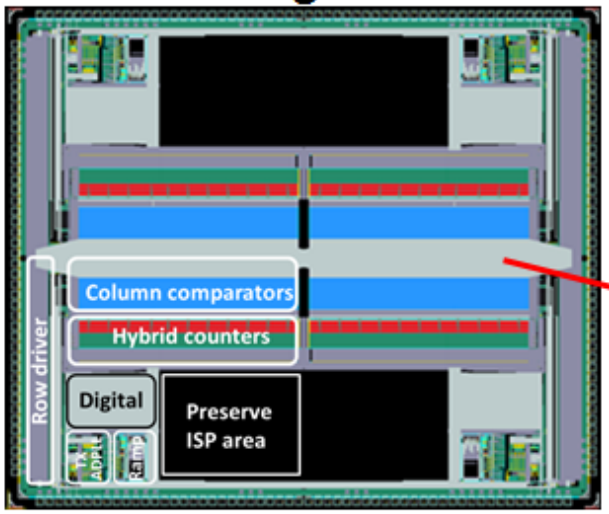


8.3mp (unit 1ch)
~=4k2k

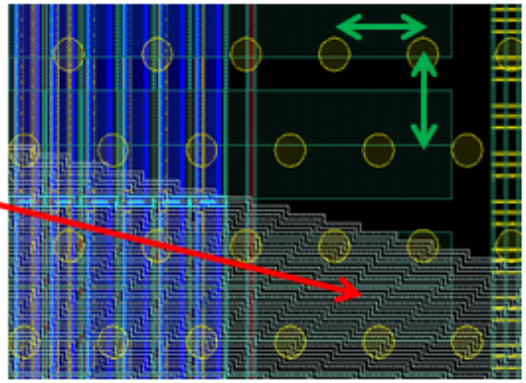
33mp (4ch)
~=8k4k
(seamless)

133mp (16ch)
~=16k8k (seamless)

1P5M Logic wafer



3D connection pitch



River routing method

same frame rate
low driving power
circuit reusable

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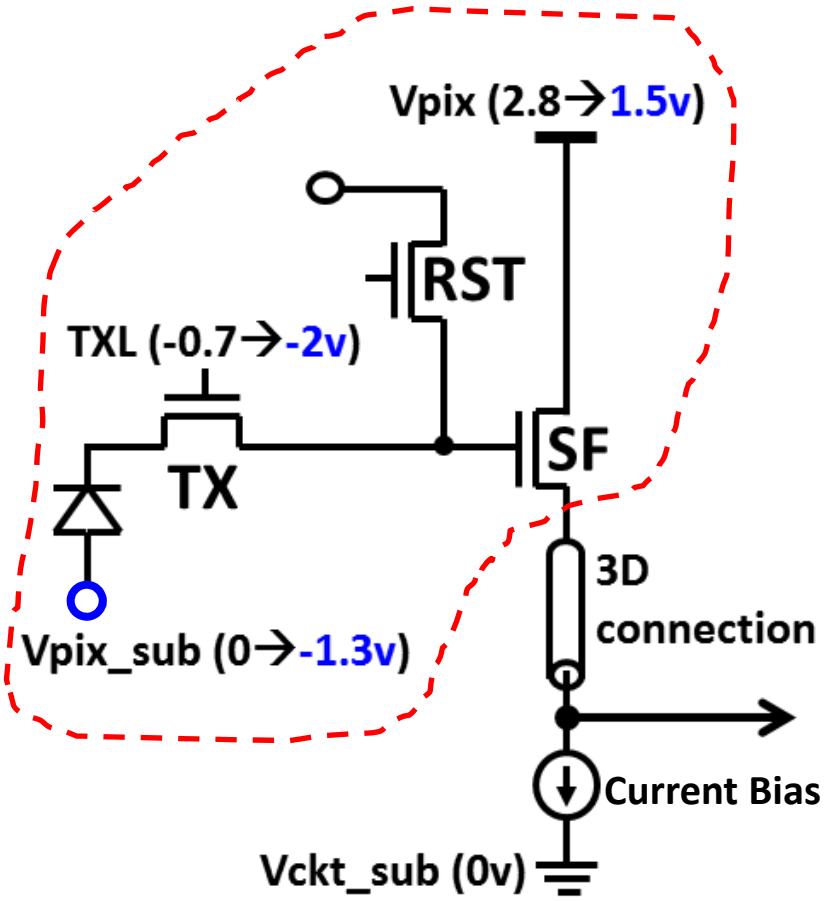
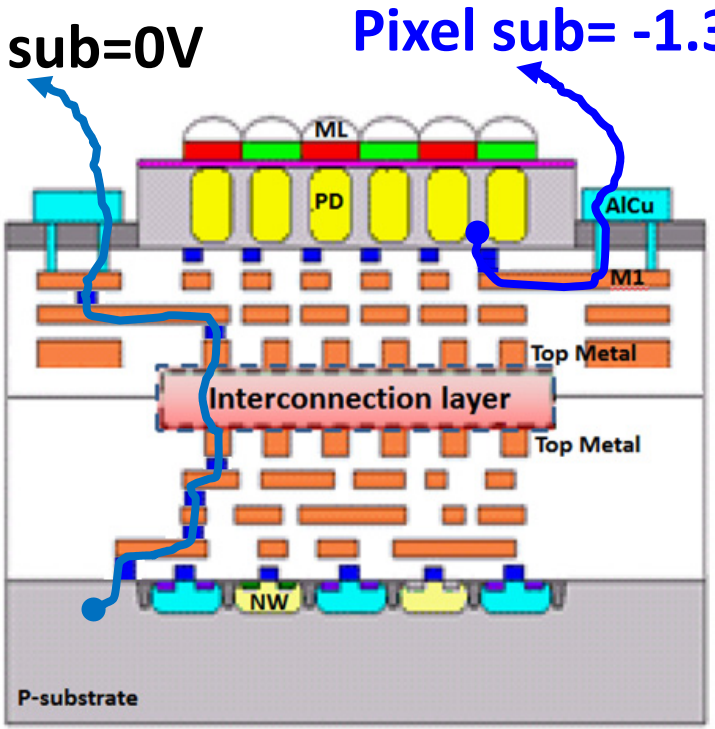
Negative Pixel Substrate Bias

Another 3D CIS Advantage: Separate Circuit & Pixel substrates





Use Negative Pixel Substrate and shift related pixel voltage equally:

1. Only non-ideal current bias may induce linearity loss
2. Vpix to 1.5v saves 46% power

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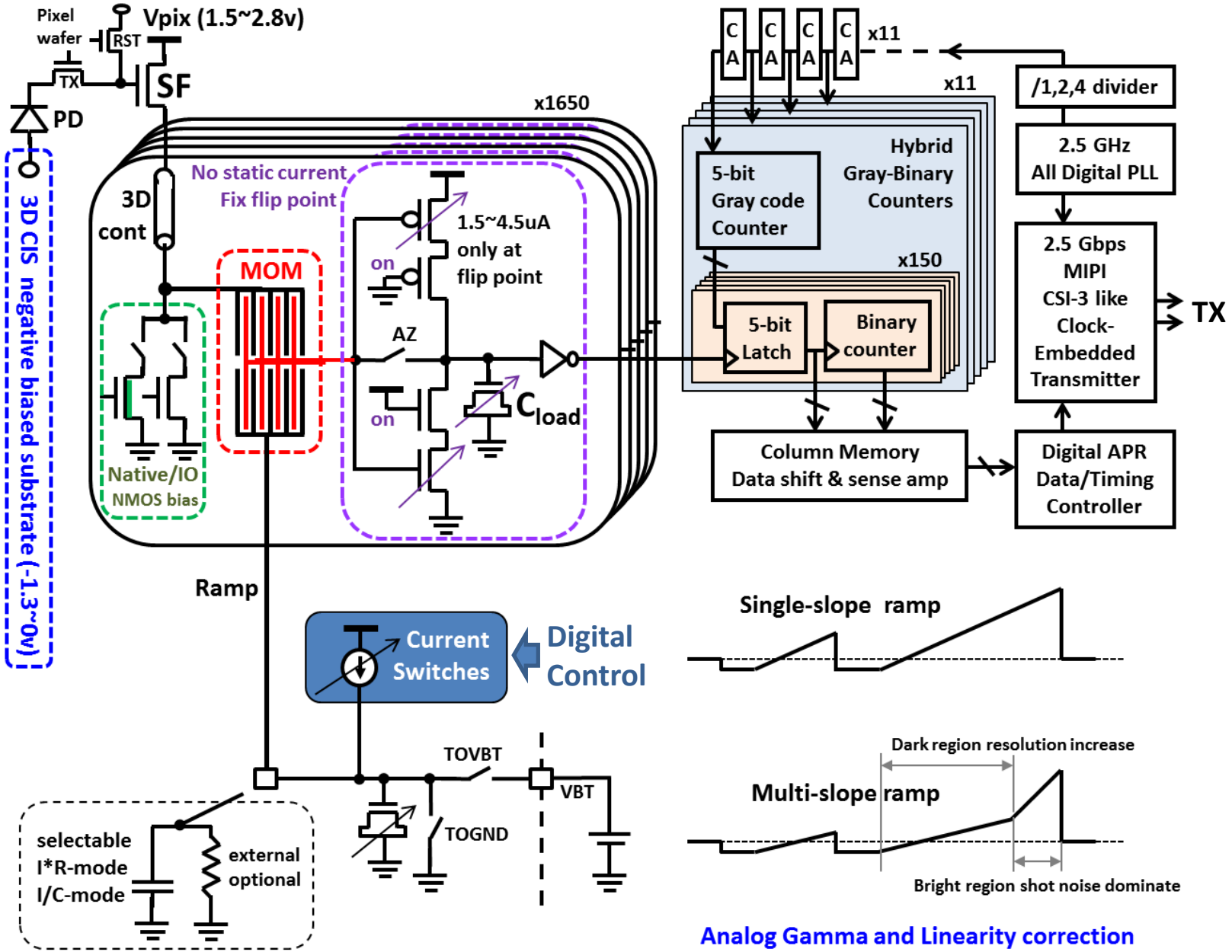
Digital-Oriented CIS Architecture



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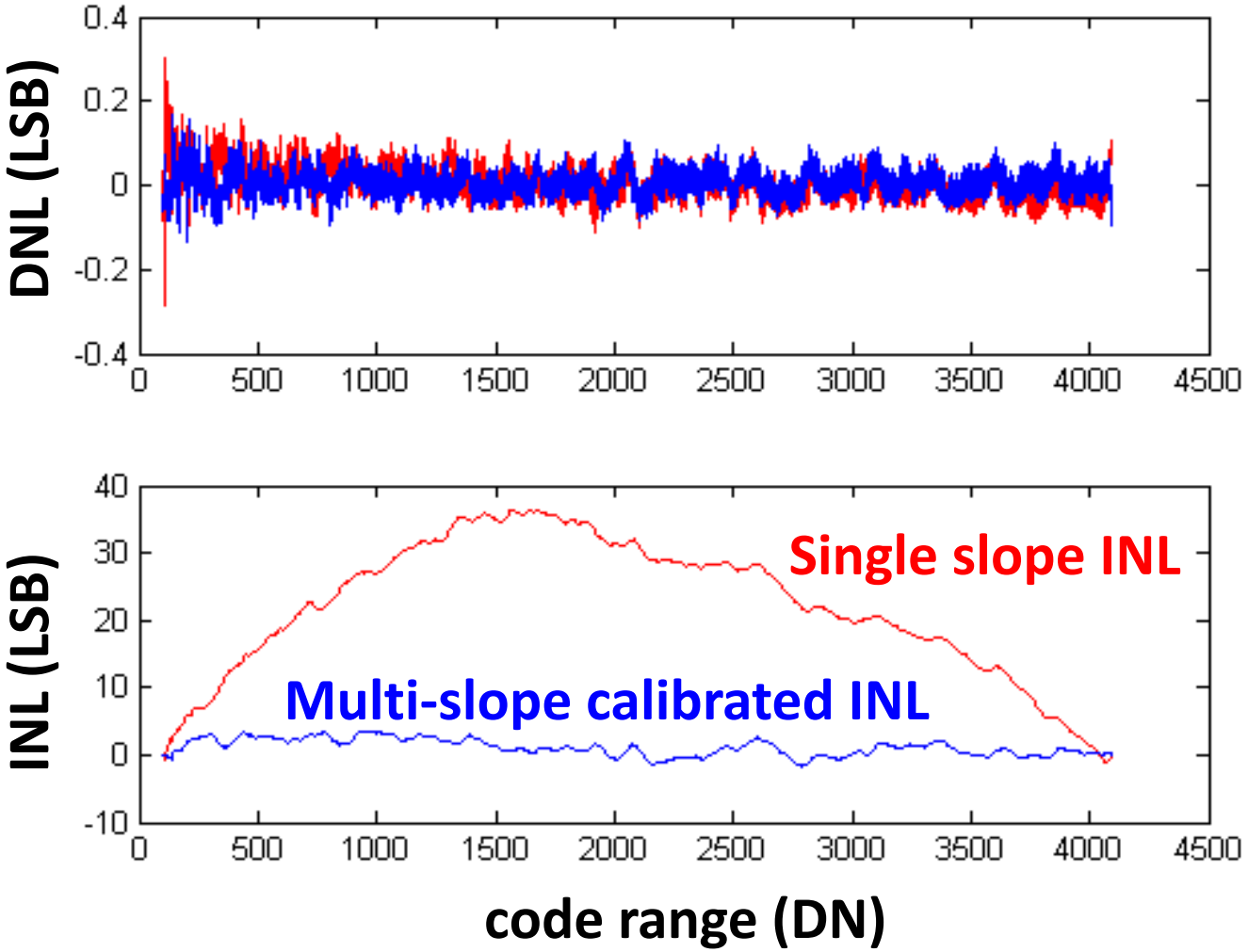
Linearity Calibration by Multi-Slope



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Analog Gamma Adjusted by Multi-Slope

Single-Slope

Multi-Slope

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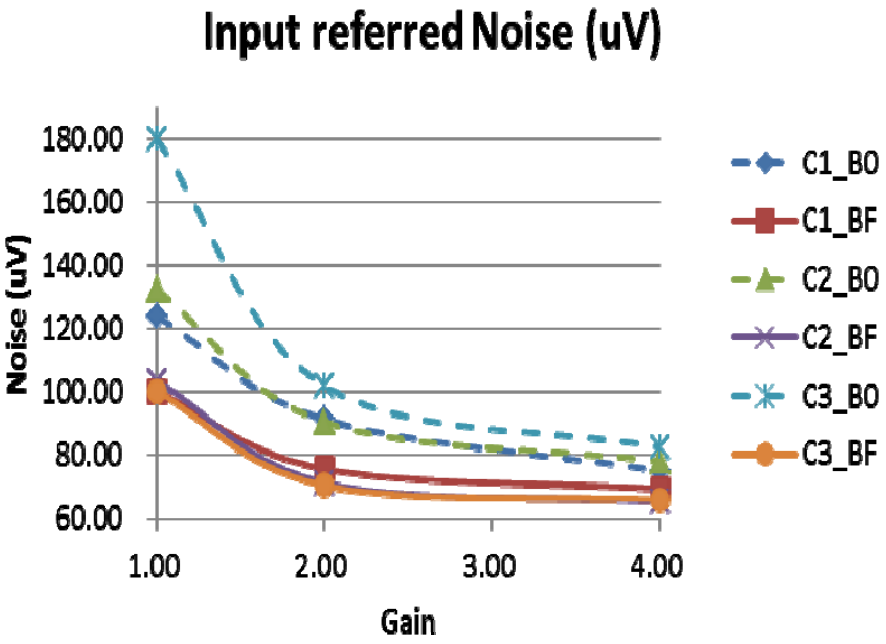
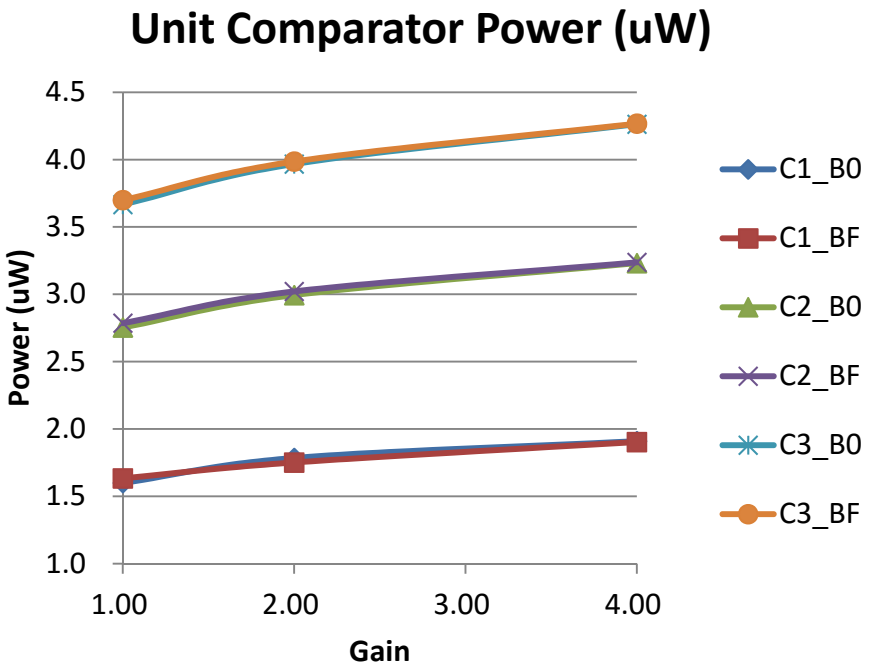
Comparator tuning for Noise & Power





Gain	CF (uV/DN)
1.00	169.49
2.00	87.72
4.00	44.05

Cx : Comparator gm Strength (x=1,2,3)

_B0 : minimum Load Capacitor for comparator

_BF : Maximum Load Capacitor for comparator

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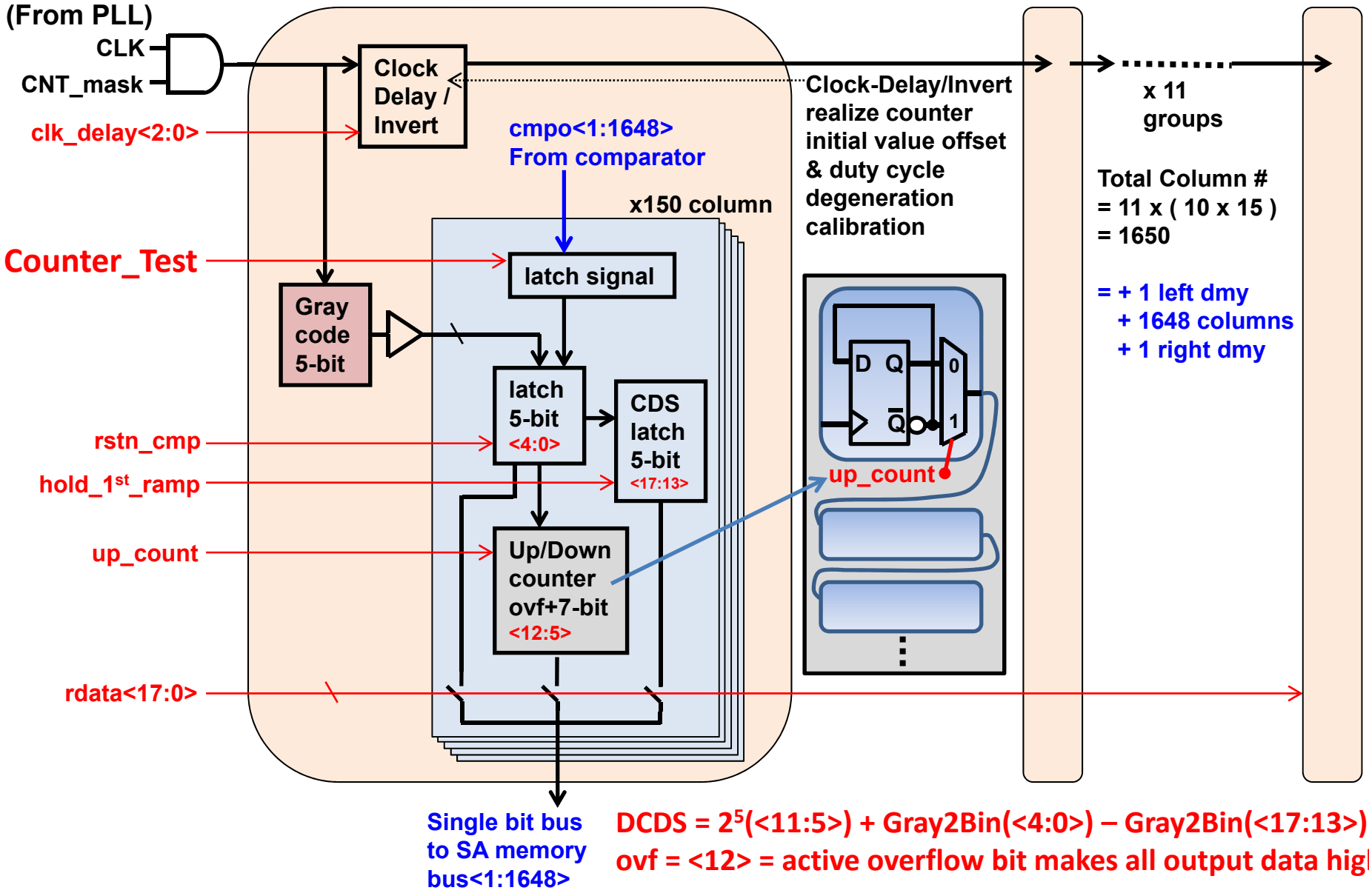
Hybrid Counter Building Blocks



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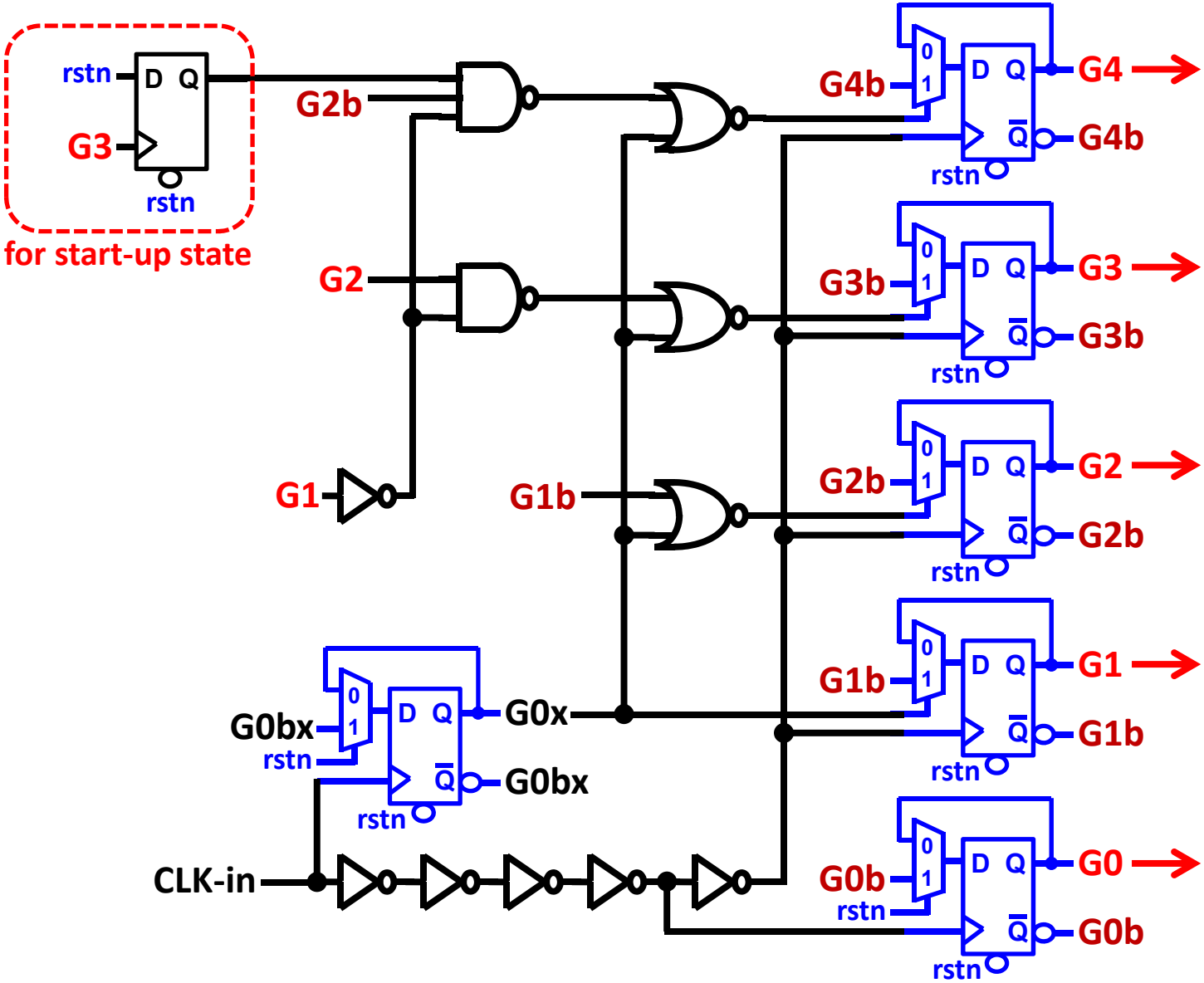
Dual Edge 5-bit Gray Code Counter

G4	G3	G2	G1	G0	DN
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	1	2
0	0	0	1	0	3
0	0	1	1	0	4
0	0	1	1	1	5
0	0	1	0	1	6
0	0	1	0	0	7
0	1	1	0	0	8
0	1	1	0	1	9
0	1	1	1	1	10
0	1	1	1	0	11
0	1	0	1	0	12
0	1	0	1	1	13
0	1	0	0	1	14
0	1	0	0	0	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	1	18
1	1	0	1	0	19
1	1	1	1	0	20
1	1	1	1	1	21
1	1	1	0	1	22
1	1	1	0	0	23
1	0	1	0	0	24
1	0	1	0	1	25
1	0	1	1	1	26
1	0	1	1	0	27
1	0	0	1	0	28
1	0	0	1	1	29
1	0	0	0	1	30
1	0	0	0	0	31



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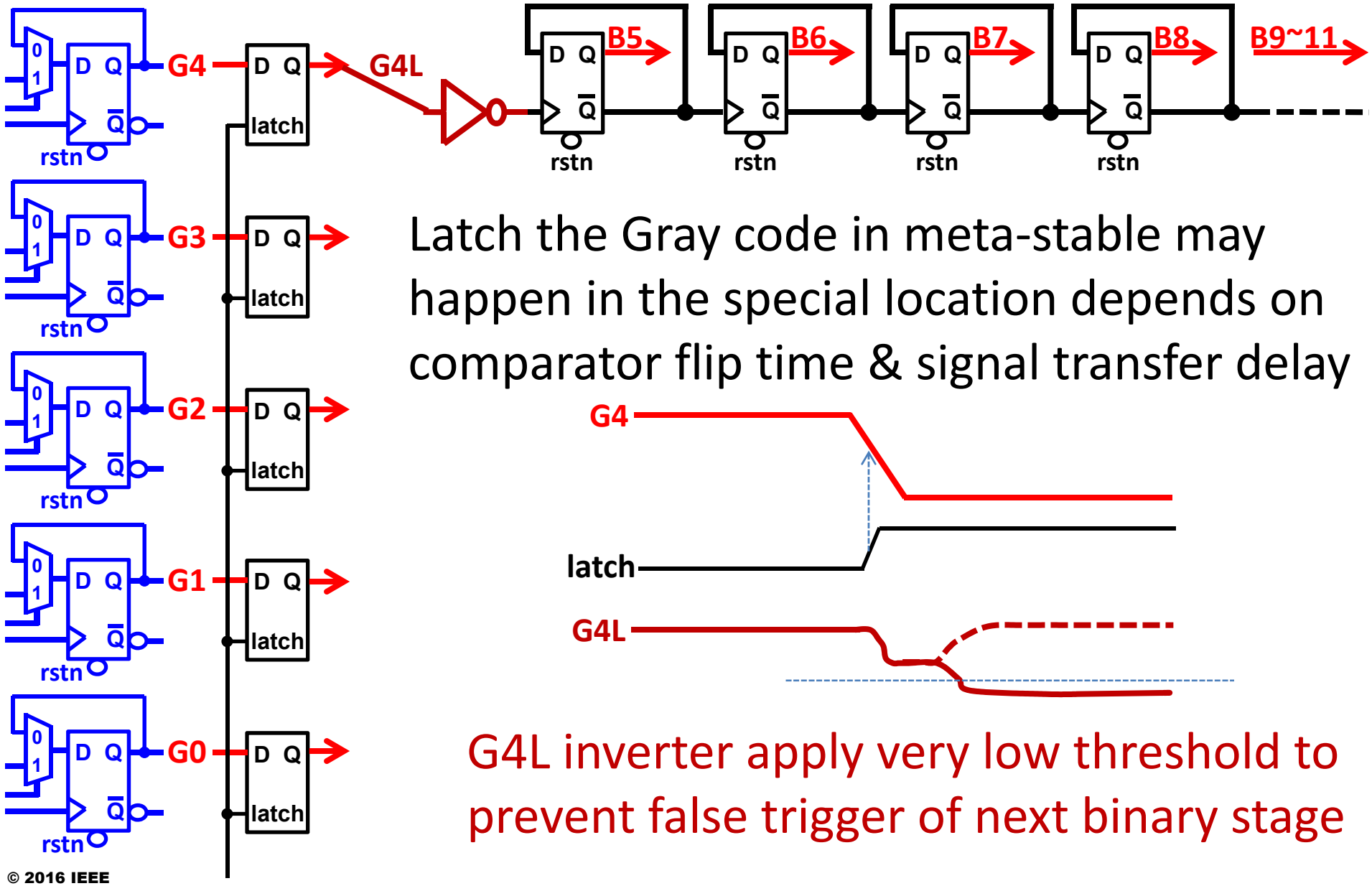
Interface issue between Gray & Binary



Latch the Gray code in meta-stable may happen in the special location depends on comparator flip time & signal transfer delay

G4L inverter apply very low threshold to prevent false trigger of next binary stage

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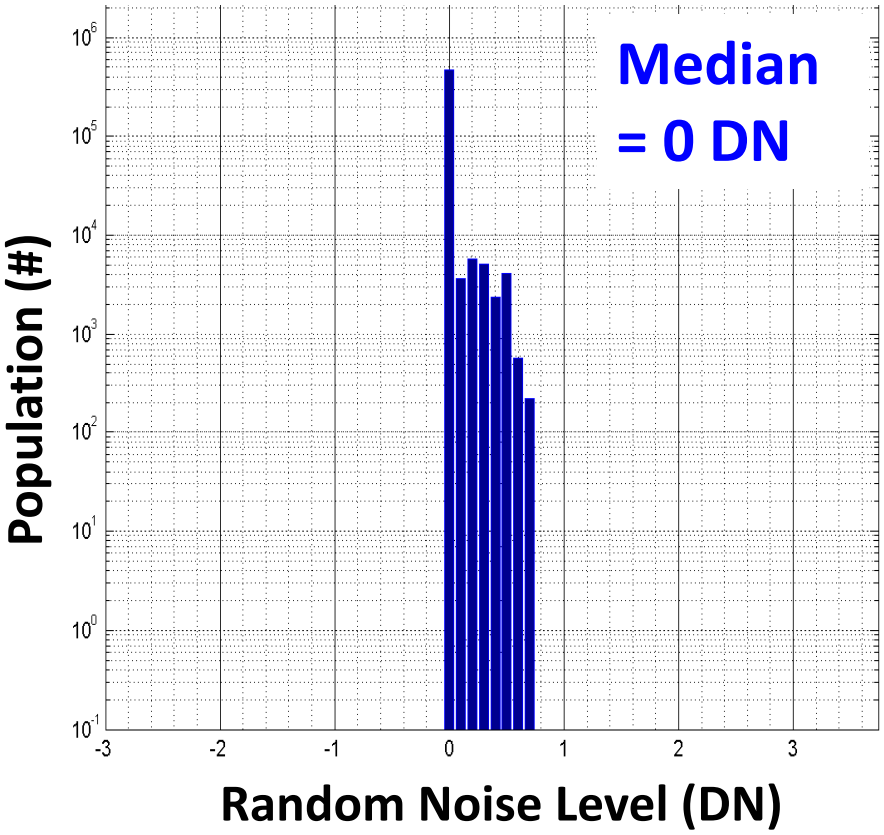
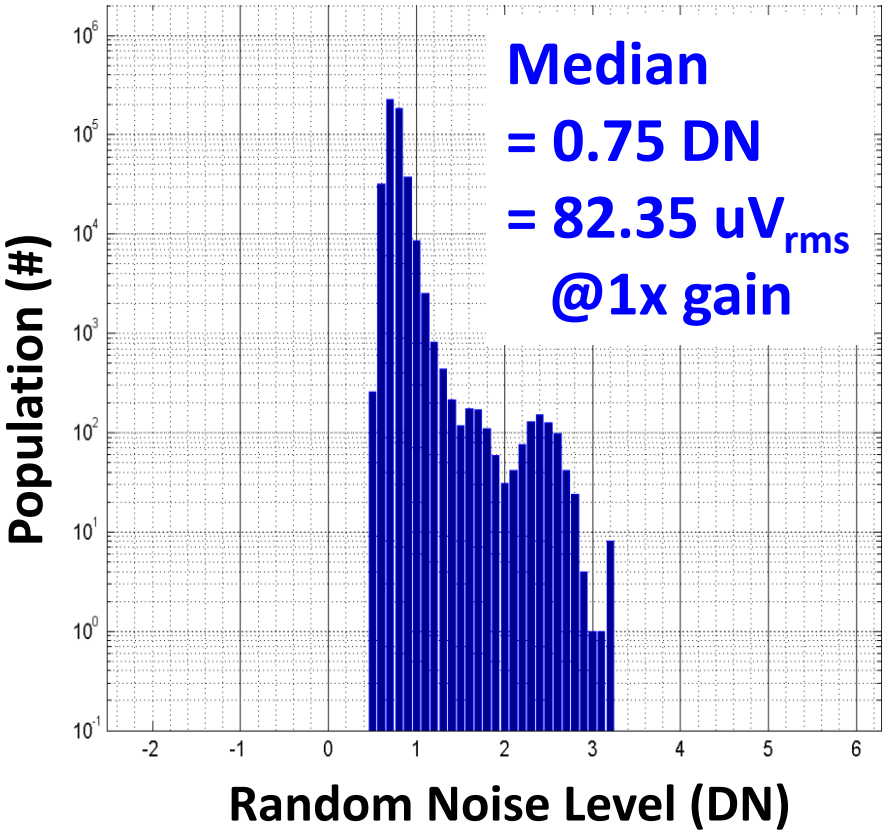
Counter/Comparator input Random Noise

Counter-in RN Histogram



Comparator-in RN Histogram



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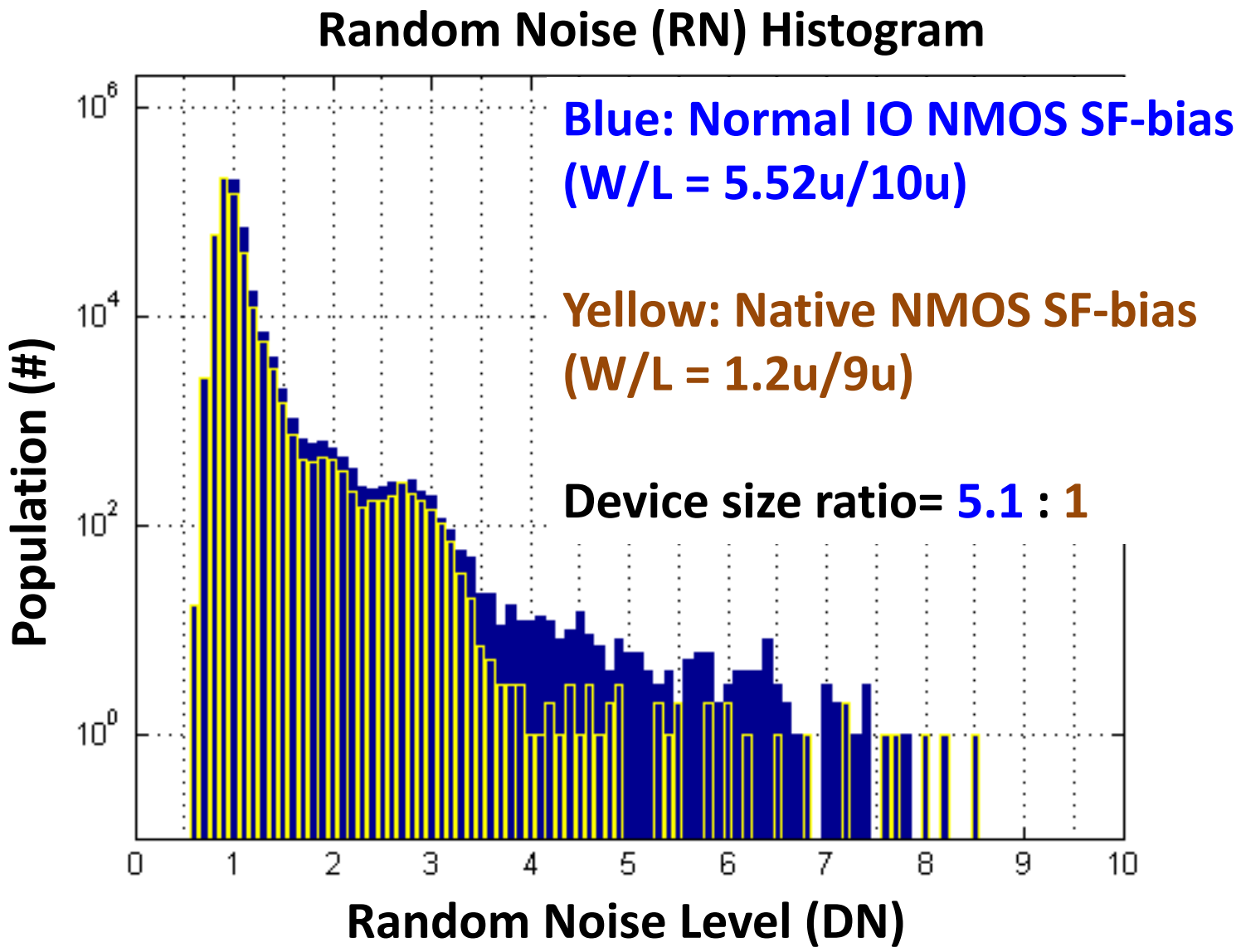
Source Follower included Random Noise



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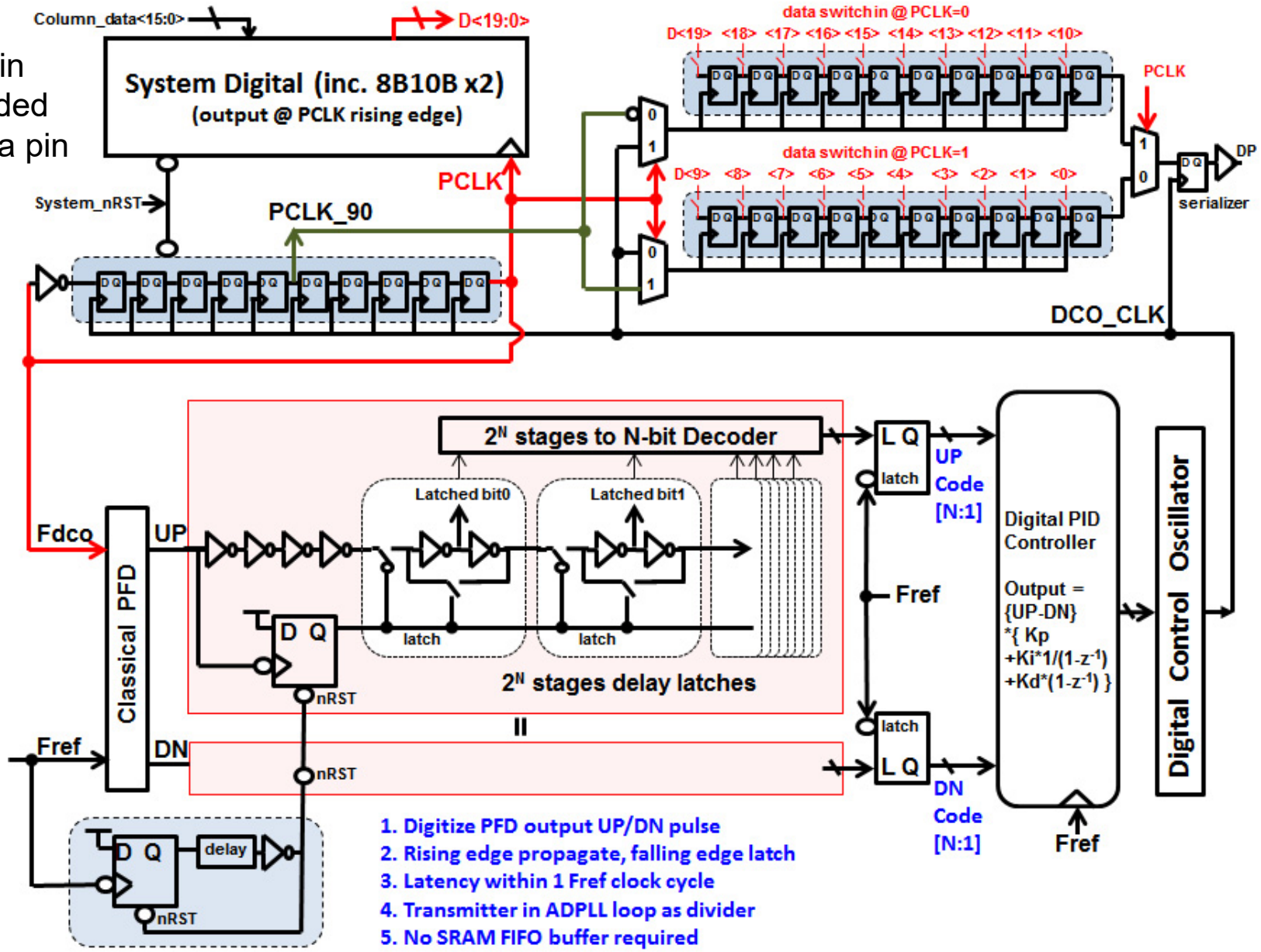
CE-Transmitter integrated in All-Digital PLL

CE:
Clock pin
Embedded
into data pin



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Specification & Performance comparison

	8Mpixel comparison		This Work			Larger Mpixel comparison	
	[3]	[4]	Prototype (2D)	unit (3D)	whole chip (3D)	[5]	[6]
Pixel count	8 mp	8.08 mp	8.28 mp	8.28 mp	33 mp	20 mp	133 mp
Technology	90nm 1p4m 2D	65nm 1P7M 3D TSV	65nm 1P5M 2D	65nm 1P5M 3D connection under array		65nm 1P7M 3D TSV	0.18um 1P4M 2D
Image size	1/3.2 inch	1/4 inch	1/4 inch	1/4 inch	1/2 inch	1/1.7 inch	1.7 inch
resolution (full frame)	N/A	3280 x 2464	3296 x 2512	3296 x 2512	6592 x 5024	5256 x 3934	15488 x 8776
Supply Voltage	N/A	2.7 V / 1.05 V	2.8 V / 1.2 V	1.5 V (up to 2.8 V) / 1.2 V		2.9 V/1.8 V/1.1 V	3.3 V / 1.8 V
ADC architecture	Pseudo Multiple Sampling	Single Slope	Single Slope, Single-Ended			Single Slope, Multiple Sampling	32-shared SAR ADC x 484
ADC resolution	10 bit	10 bit	12 bit			12 bit	12 bit
Readout ckt. Random Noise	134 uVrms (M=16)	139 uVrms (18dB Again)	83.4 uVrms (1x Again)	82.35 uVrms (1x Again)		99.6 uVrms (27dB, M=2)	281.6 uVrms (3x PGA gain)
Frame rate (full frame)	15 fps	30 fps	15 / 7.5 fps*	15 / 7.5 fps*		30 fps	60 fps
Data rate (full frame)	130 MHz parallel	750 Mbps serial 4 lane + clk lane	896/448 Mbps* serial 2 lane + clk lane	2.5/1.25 Gbps* serial 1 lane clk-embedded	2.5/1.25 Gbps* serial 4 lane clk-embedded	2.3 Gbps serial 8 lane clk-embedded	1.15 Gbps 112 lane + clk lane
Power (full frame)	280 mW	185 mW	52mW	45 mW	180 mW	532 mW	11000 mW
Array-to-Chip area ratio (%)	44.8 %	64.2 %	30 %	82.5 %		67.8 %	43.9 %

* Note: Subject to FPGA receiver development & PCB signal integrity status, all measured data operate at half speed for better stability.

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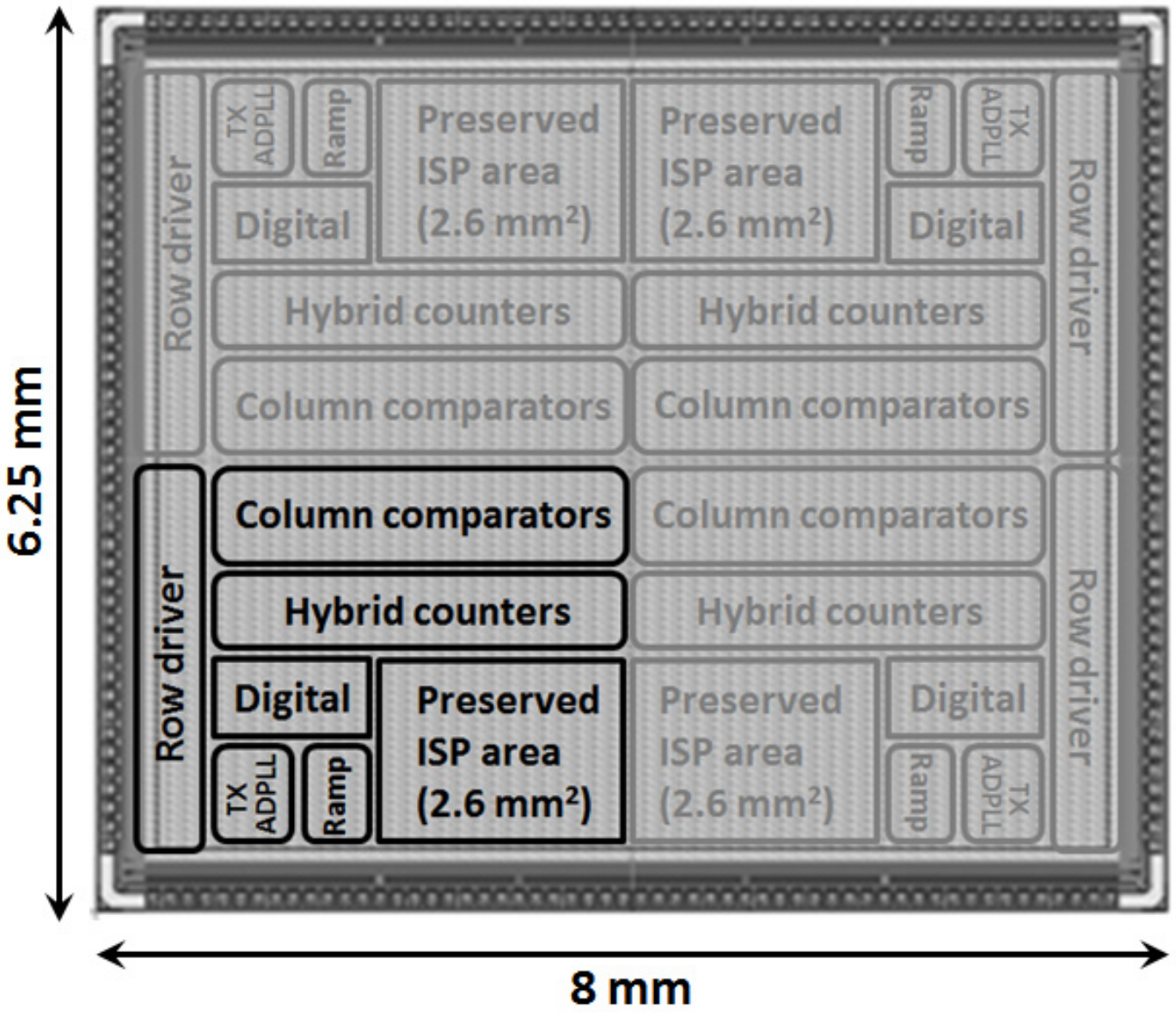
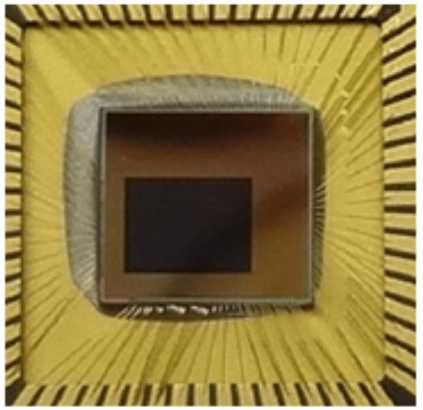
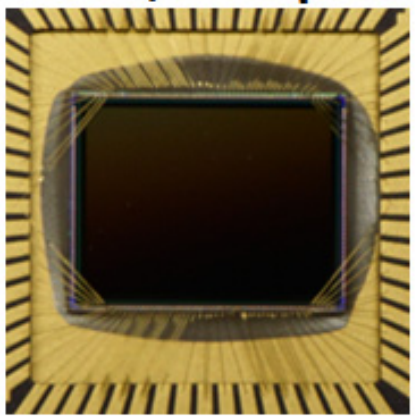
Chip Photograph with 68-pin CLCC package



2D, 8.3Mpixel



3D, 33Mpixel



17-pin/unit

Total 17 x 4 = 68-pin

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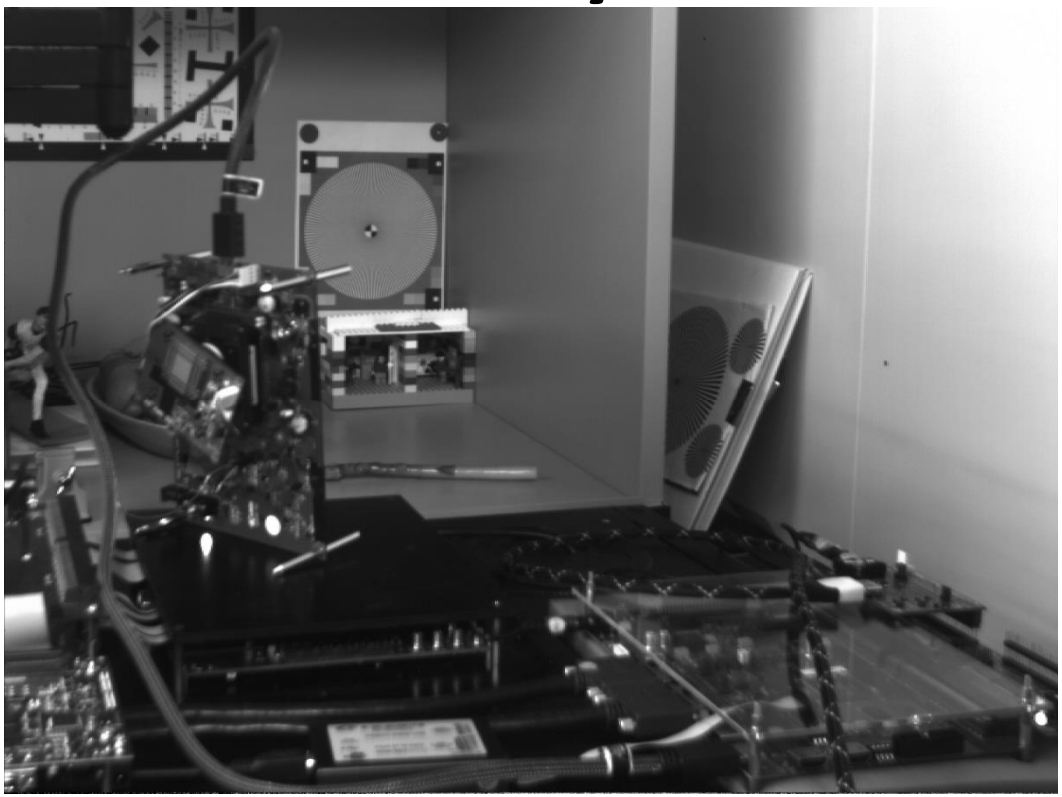
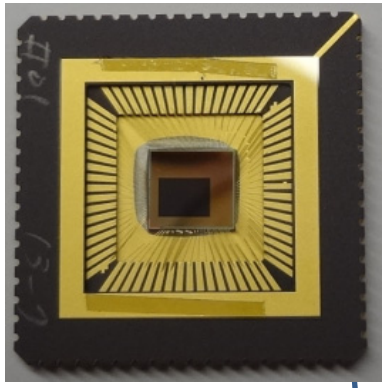
System Environment

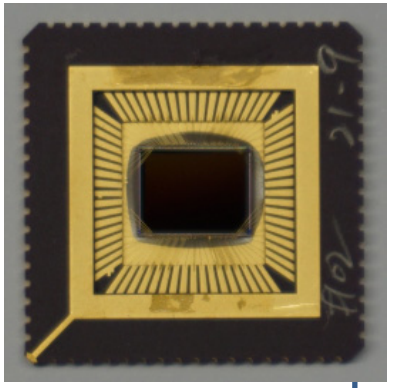


Both use same sensor circuits except TX & MOM cap

2D BSI (8.3mp)



3D stacked (33Mp)



MIPI CSI-2 like
(1clk+2data lane)

TI DeSerializer

Parallel
Single-to-Diff

HDMI cable
includes all
4 lanes + Pwr + I2C

PC

Camera Link to PC

USB

PC-to-FPGA
Program BOX

Xilinx
K7(TRX)
FPGA

HDMI connector

MIPI CIS-3 like (8b10b)
Clock Embedded
4 lanes for 4 channels

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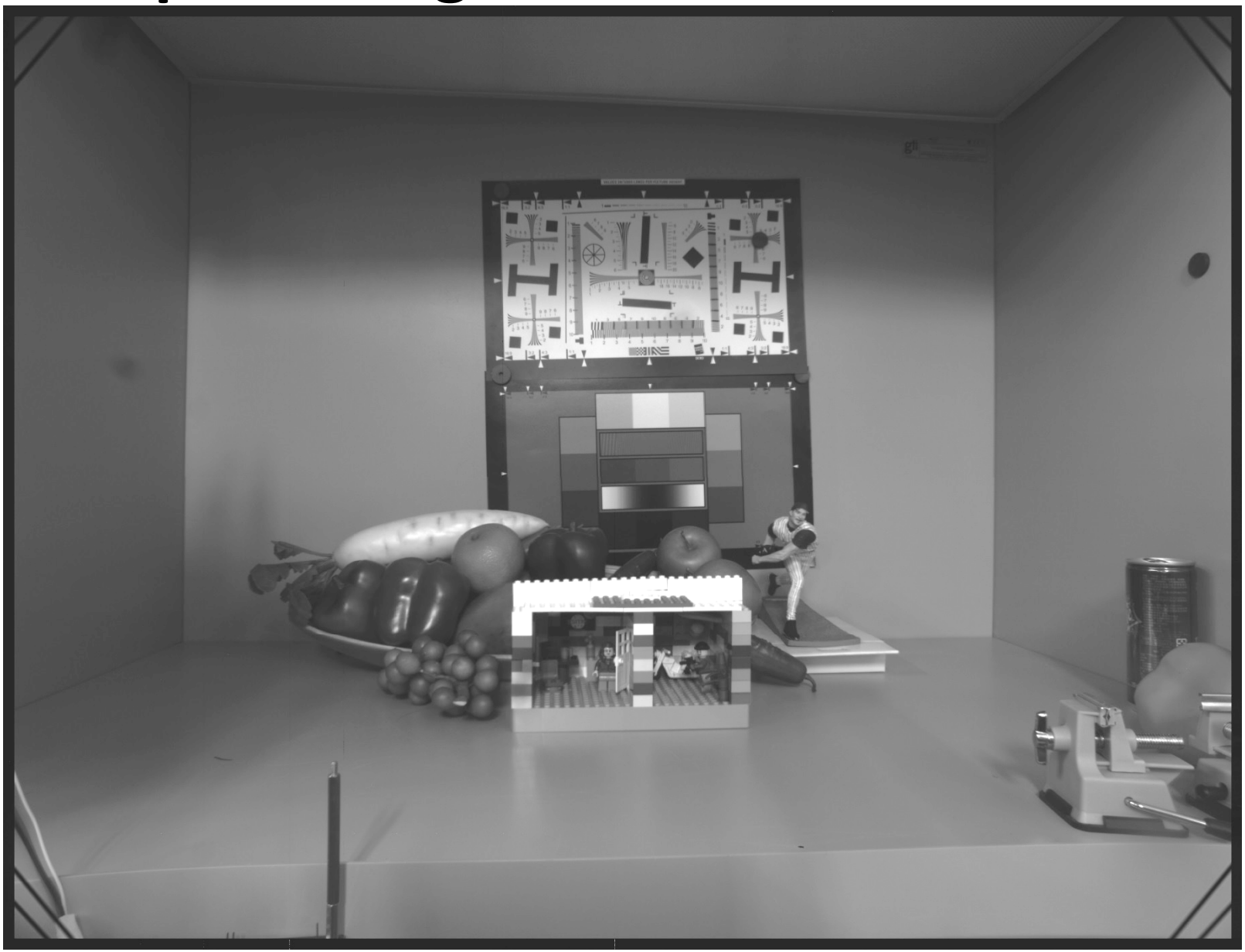
33Mpixel Image (@ Vpix/PixSub/TXL=1.5/-1.3/-2v)

Bond wire shadow at 4 corners of 33 Mpixel image.



No discrepancy at unit boundary only by process uniformity

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Conclusions

By 3D-connection under pixel array & river routing, we put all circuits under array and realize scalable unit array stitch.

By negative pixel substrate bias & customized MOM cap, We can use the most advanced low voltage digital process to integrate computational imaging applications.

To accommodate the advanced digital process, we design by Digital-Oriented CIS architecture: a compact ADPLL + CE-TX, inverter based comparator, Native nmos sink, hybrid counter, multi-slope ramp to calibrate linearity & analog gamma, for a low pin#, low voltage/power, low noise, & small area unit.

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A 1.1μm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-to-Digital Converters

Toshiki Arai[1], Toshio Yasue[1], Kazuya Kitamura[1], Hiroshi Shimamoto[1], Tomohiko Kosugi[2], Sungwook Jun[2], Satoshi Aoyama[2], Ming-Chieh Hsu[3], Yuichiro Yamashita[3], Hirofumi Sumi[3], and Shoji Kawahito[2,4]

[1] NHK Science & Technology Research Laboratories, Tokyo, Japan
[2] Brookman Technology Inc., Hamamatsu, Japan
[3] Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan
[4] Shizuoka University, Hamamatsu, Japan

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Outline

1. Overview
   - 8K Super Hi-Vision
   - Goal in this work
2. Architecture of the BSI 3D-stacked image sensor
   - Features
   - Interconnection technology
   - ADC architecture
3. Measurement
   - Specifications
   - Performance comparison
4. Summary

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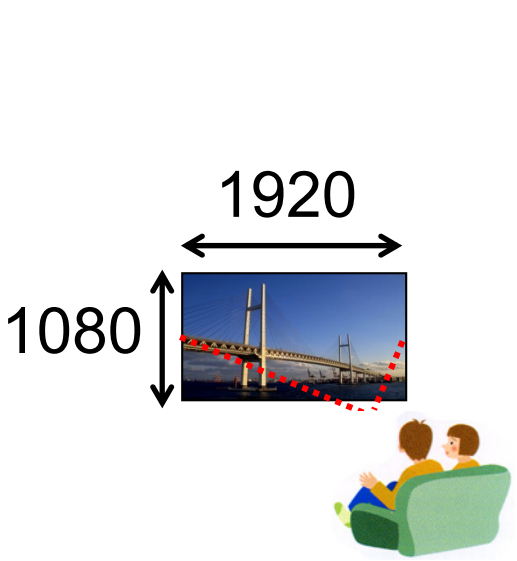
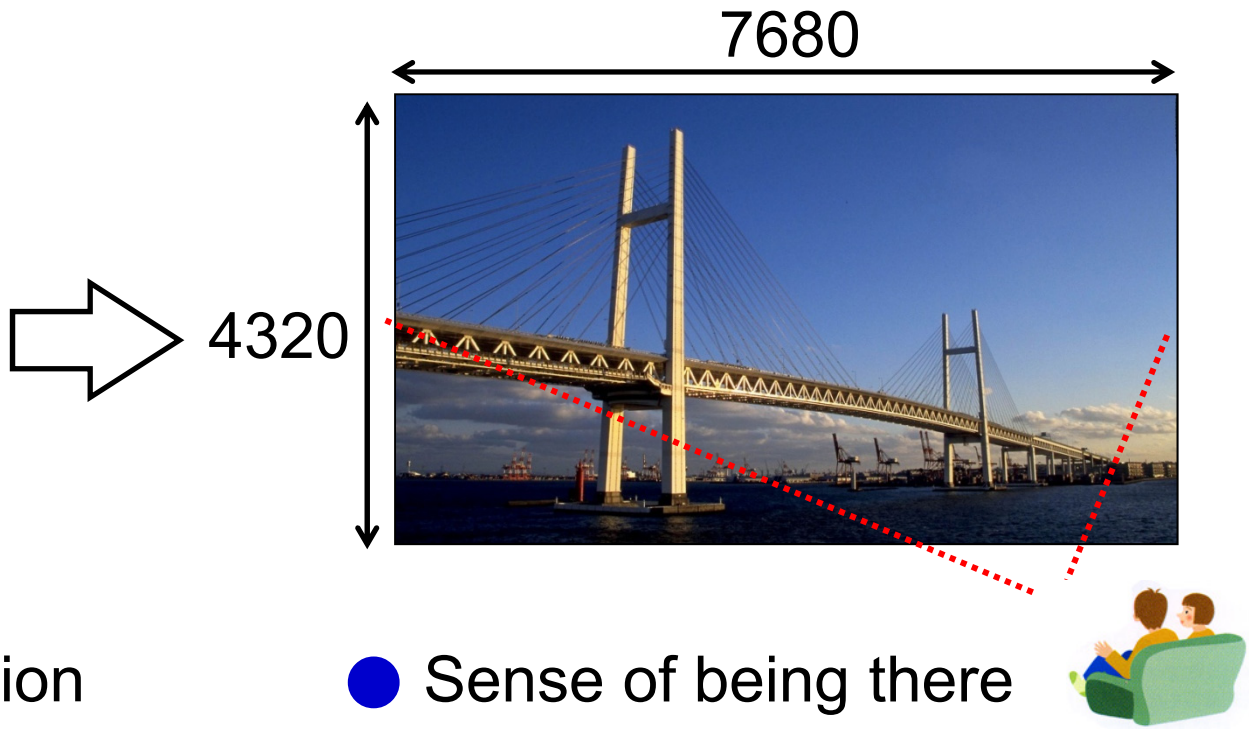
8K Super Hi-Vision (SHV)

- Next generation ultra-high definition TV system

HDTV (2Mpixel)

8KSHV (33Mpixel)





HDTV: High definition television

- Sense of being there
- Sensation of realness

- 8K broadcasting will start by 2018 in Japan

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Video parameters of 8K Super Hi-Vision

- Underlined high-end values are for "Full-spec SHV"

	ITU-R BT.2020 (Excerpt)
Pixel number (H×V)	7680×4320, 3840×2160
Frame frequency	120 Hz, 100 Hz, 60 Hz, …
Scan mode	Progressive
Colorimetry	Wide color gamut
Bit depth	12 bit, 10 bit

Standardized in Rec. ITU-R BT. 2020, SMPTE ST 2036-1, and ARIB STD-B56

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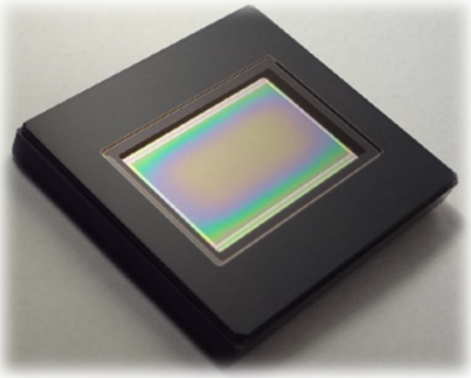
Our previous work

- First developed a 33Mpixel 120fps CMOS image sensor with a 12-bit column-parallel 2-stage (first 4 bits, second 8 bits) cyclic analog-to-digital converter (ADC)



K. Kitamura, et al.,
IEEE Trans. Elec. Dev., p. 3426 (2012)

- 8K SHV prototype camera with 3 CMOS sensors for “Full-spec SHV”

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Goal in this work

- Small 8K SHV camera with 3 CMOS sensors

Super 35 mm (1.7 inch)

Small

- High frame rate
- High sensitivity for small pixels
- Deep depth of field

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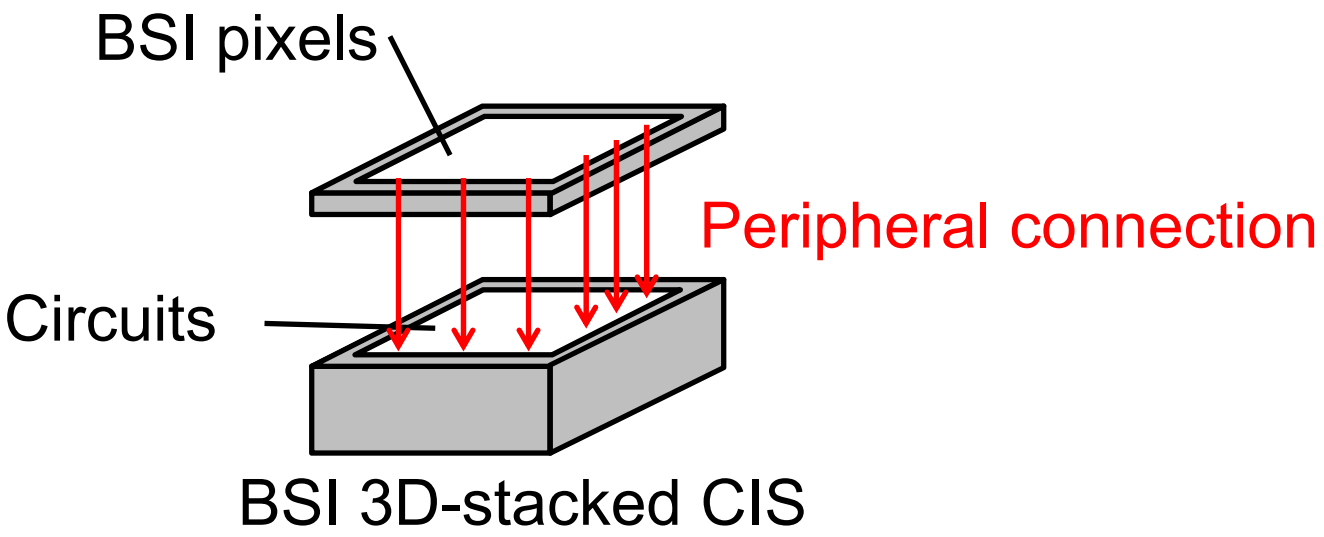
Recent CIS technology trend

- Backside illuminated (BSI) 3D-stacked CMOS image sensors



S. Sukegawa, et al., ISSCC, p. 484 (2013)

- A BSI pixel wafer and an ASIC wafer are stacked with peripheral connection

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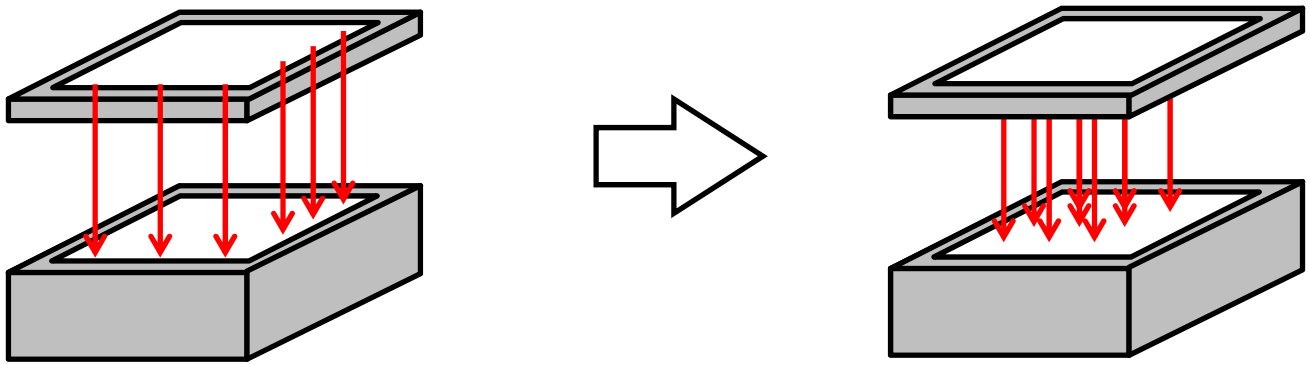
Task and tackle of 3D-stacked CIS

Task

× Conventional 3D-stacked CIS uses peripheral connection by Through-Silicon Via (TSV)

Challenge

○ 3D-stacked CIS uses interconnection technology without TSV



Peripheral connection

interconnection

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Contents

- This presentation
  - Development of a 1.1μm 33Mpixel 240fps BSI 3D-stacked CMOS image sensor
- Key technologies
  - Interconnection technology
  - 12-bit 3-stage cyclic-based ADC

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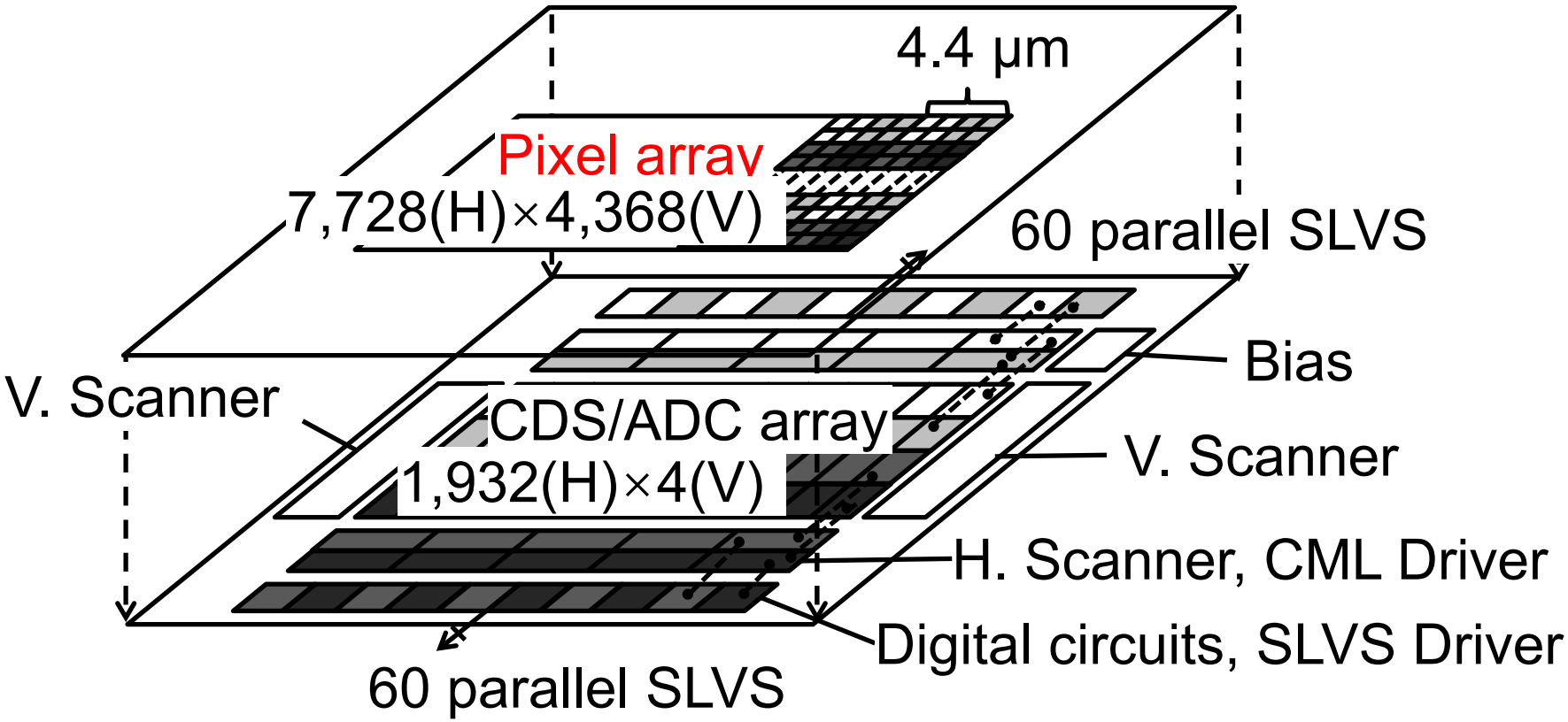
Features of the BSI 3D-stacked CIS

- Pixel count for full-spec SHV (33 Mpixel, 1.1 μm sq.)
- 12-bit 3-stage cyclic based ADC (Cyclic-Cyclic-SAR)
- BSI 3D stack (4.4-μm-pitch interconnection)



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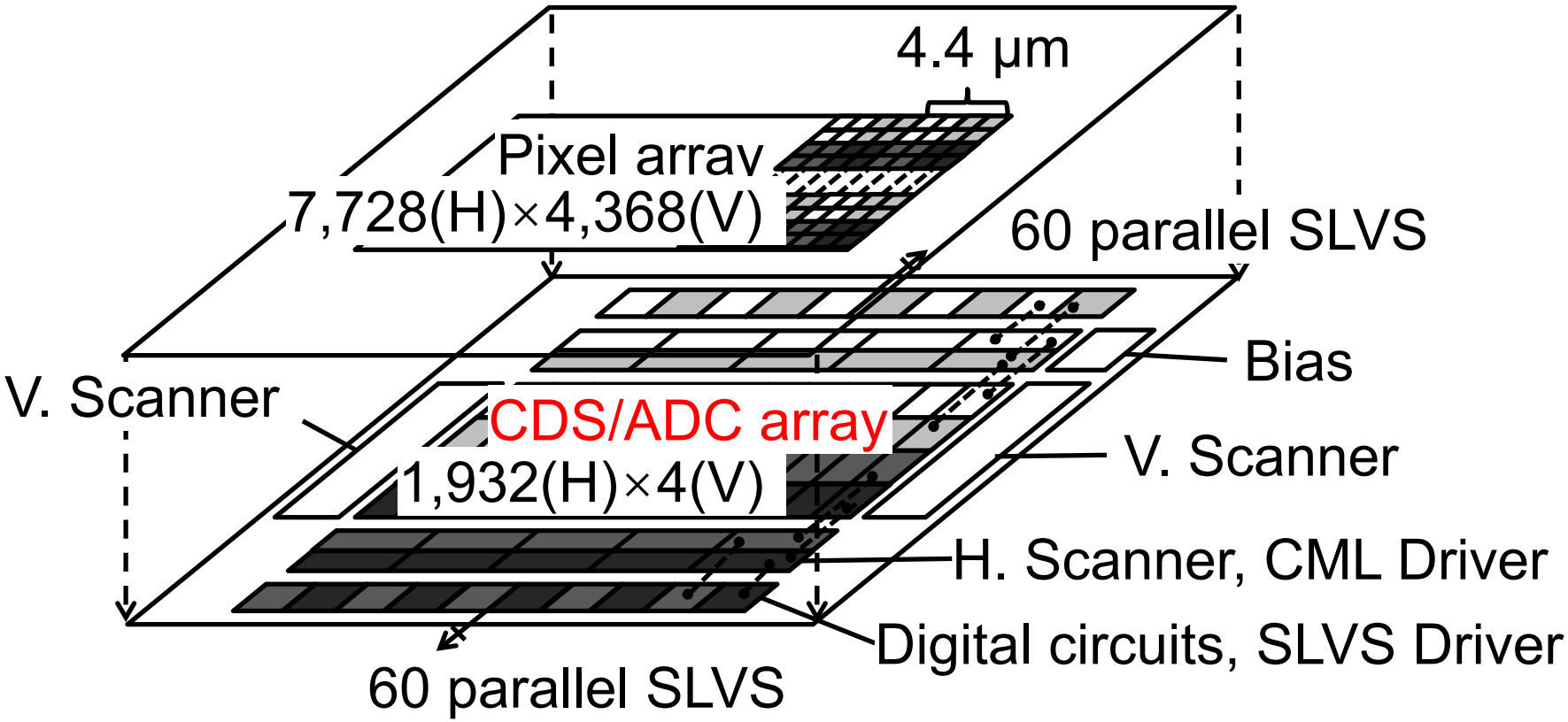
Features of the BSI 3D-stacked CIS

- Pixel count for full-spec SHV (33 Mpixel, 1.1 μm sq.)
- 12-bit 3-stage cyclic based ADC (Cyclic-Cyclic-SAR)
- BSI 3D stack (4.4-μm-pitch interconnection)



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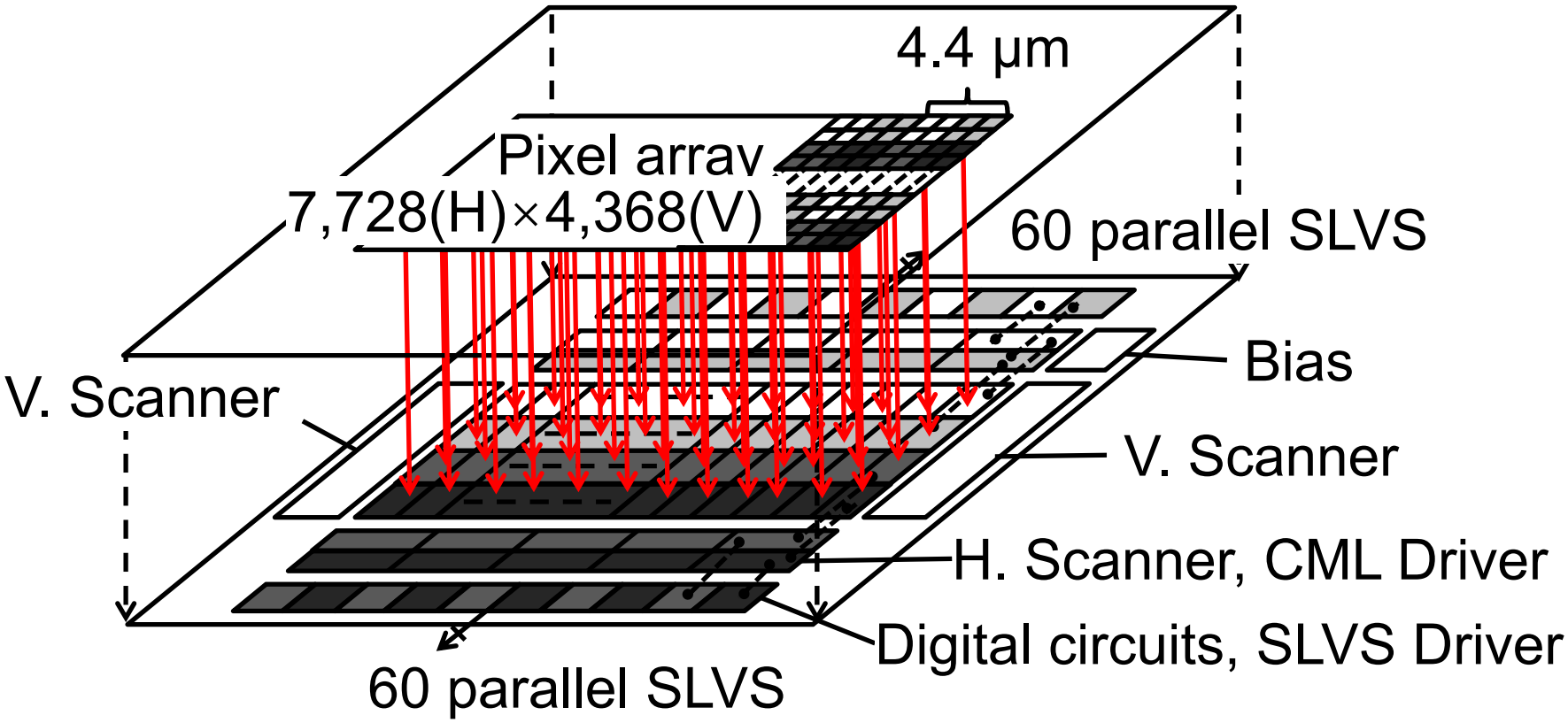
Features of the BSI 3D-stacked CIS

- Pixel count for full-spec SHV (33 Mpixel, 1.1 μm sq.)
- 12-bit 3-stage cyclic based ADC (Cyclic-Cyclic-SAR)
- BSI 3D stack (4.4-μm-pitch interconnection)



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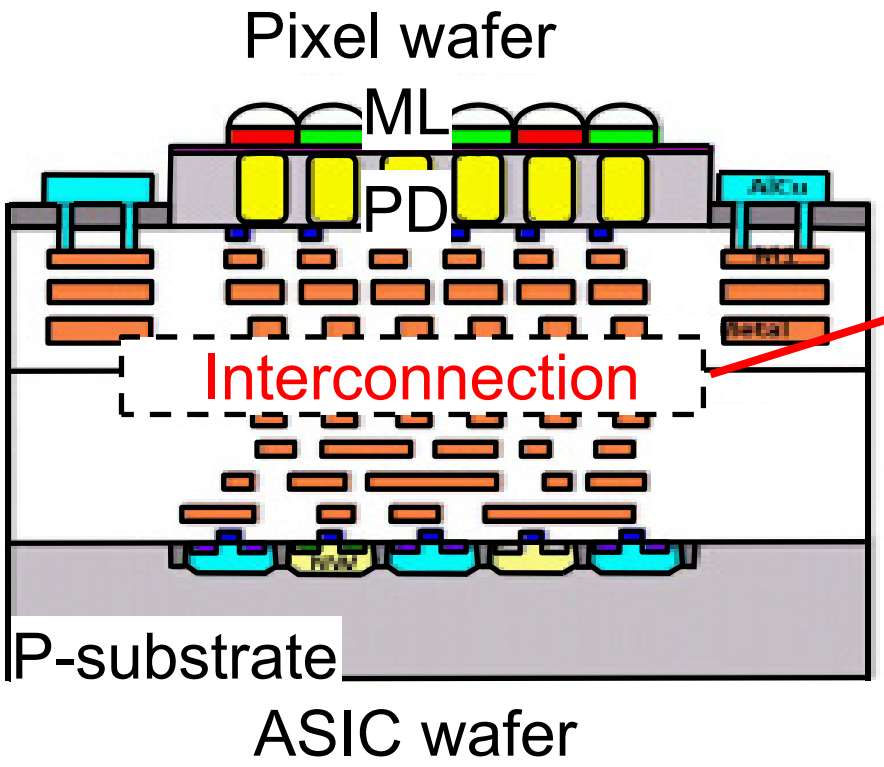
Interconnection

- The pixel wafer and the ASIC wafer are stacked face-to-face
- Both wafers are internally connected without TSV



- Metal and insulator layers are connected, respectively
- The wafers are independently tuned for each process

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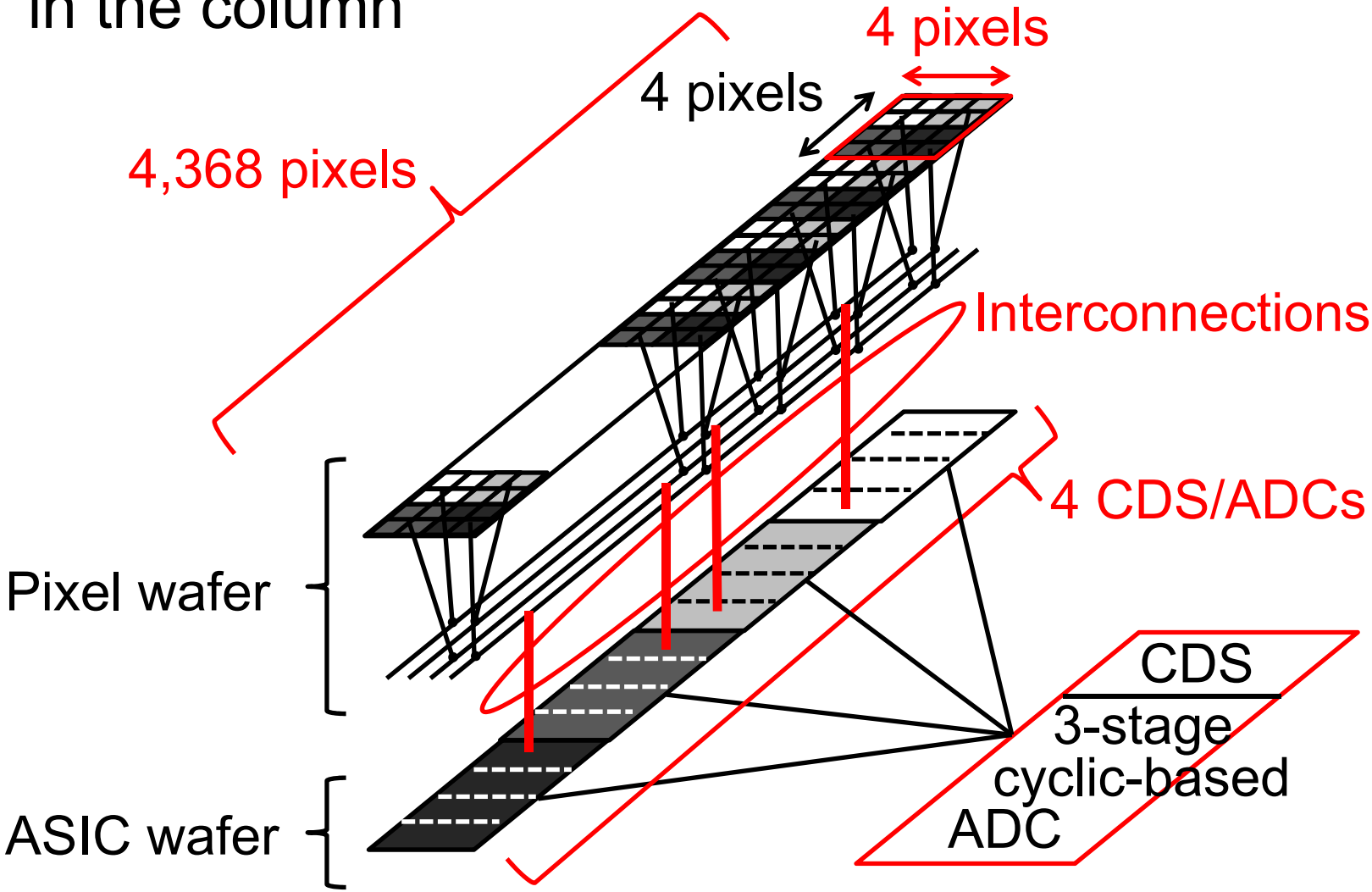
Placement of pixels, ADCs and interconnections

- 4(H)x4,368(V) pixels and 4 CDS/ADCs are overlaid in the column



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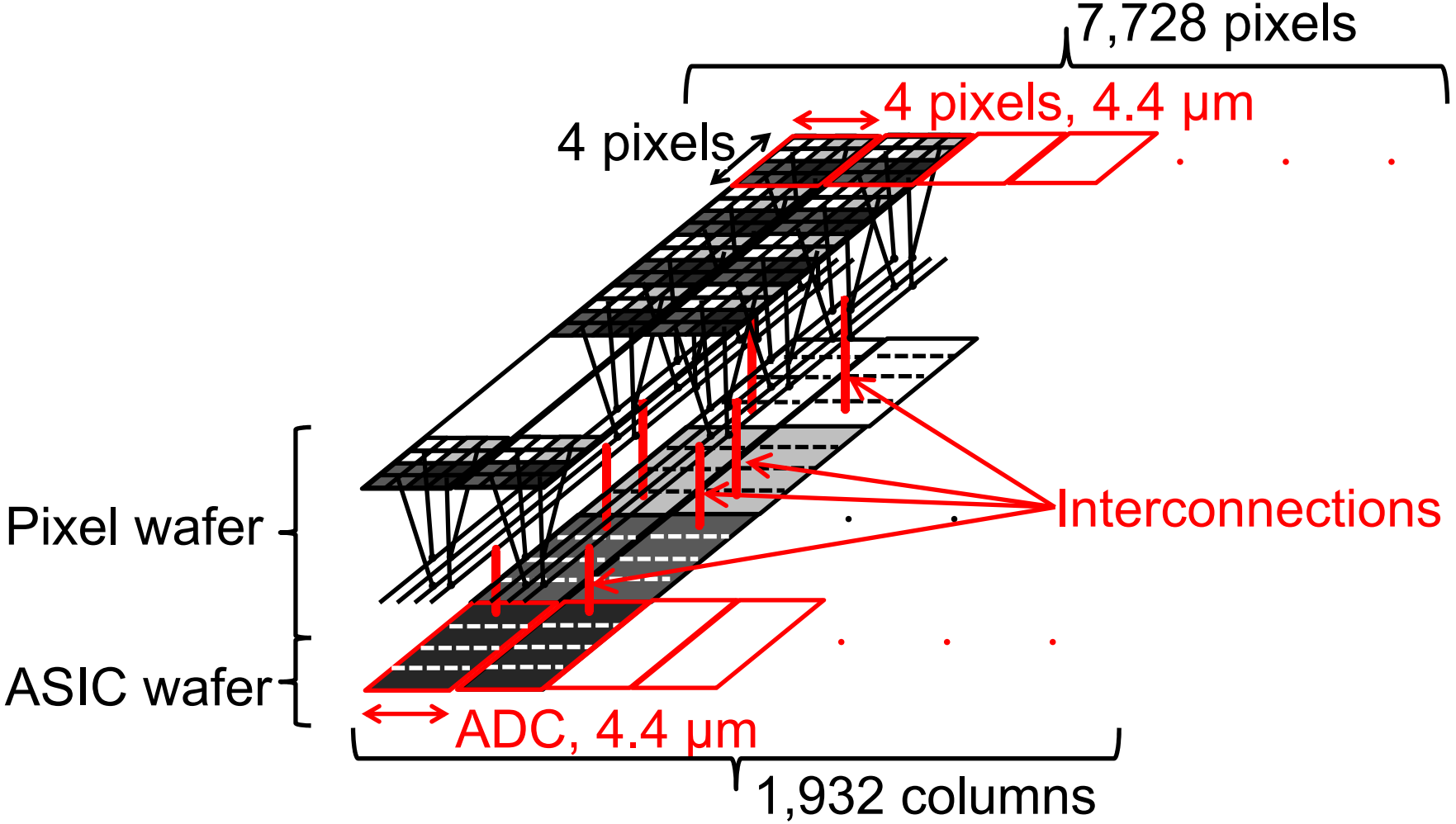
Horizontal pitch of column

- The horizontal column pitch is 4.4 μm with 4 pixels
- In total 1,932 columns and 7,728 pixels are placed



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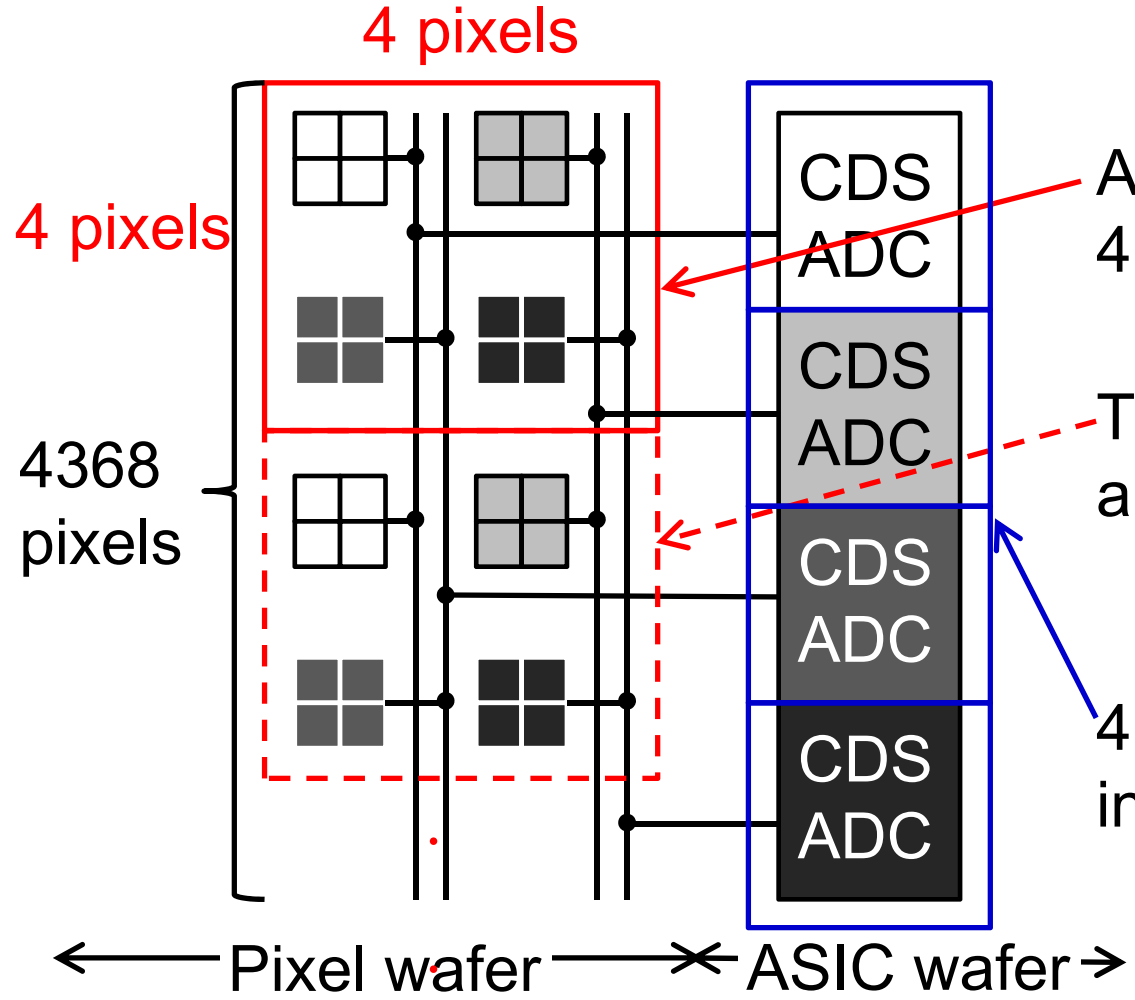
Block diagram of pixels and ADCs in column

- 4x4 pixel units repeat along the column
- 4 CDS/ADC units are placed in the column



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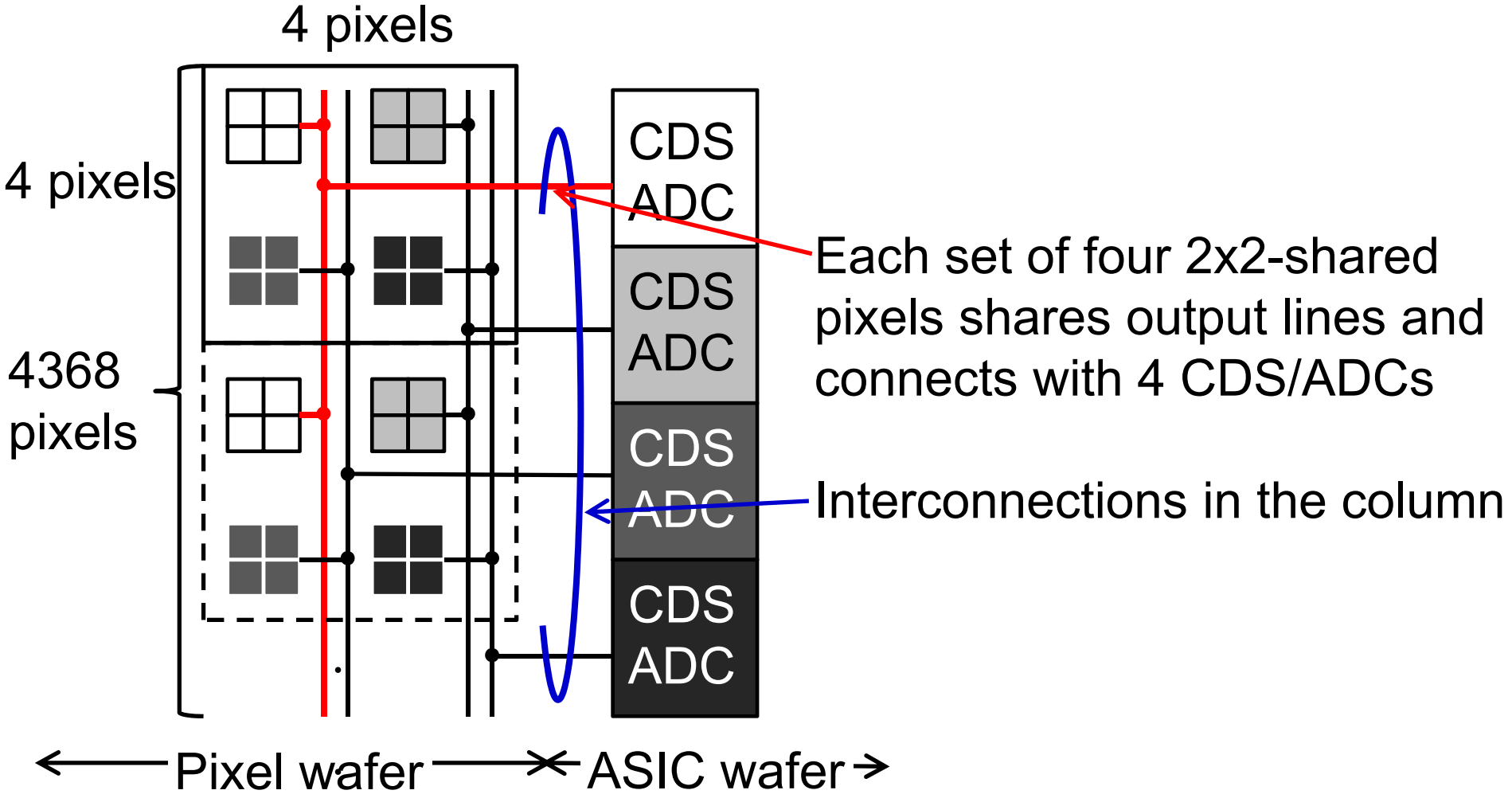
Block diagram of interconnections

- Pixels and ADCs are connected by interconnections in the column



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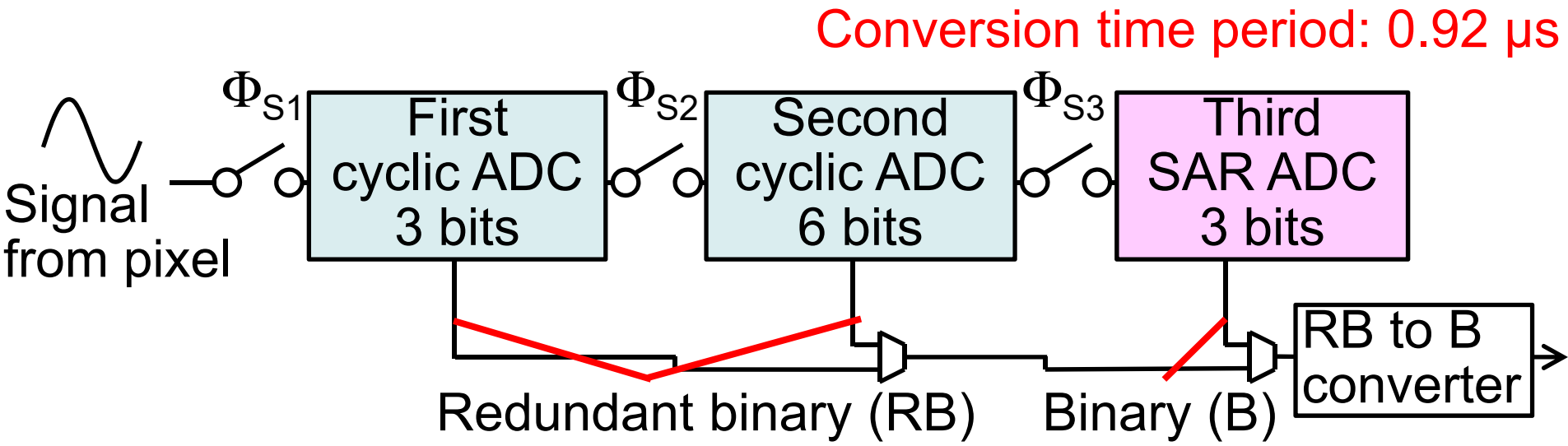
3-stage cyclic-based ADC

- 3-stage pipelined operation enables conversion time period of 0.92 µs which achieves 240 fps

- The 3-stage ADC



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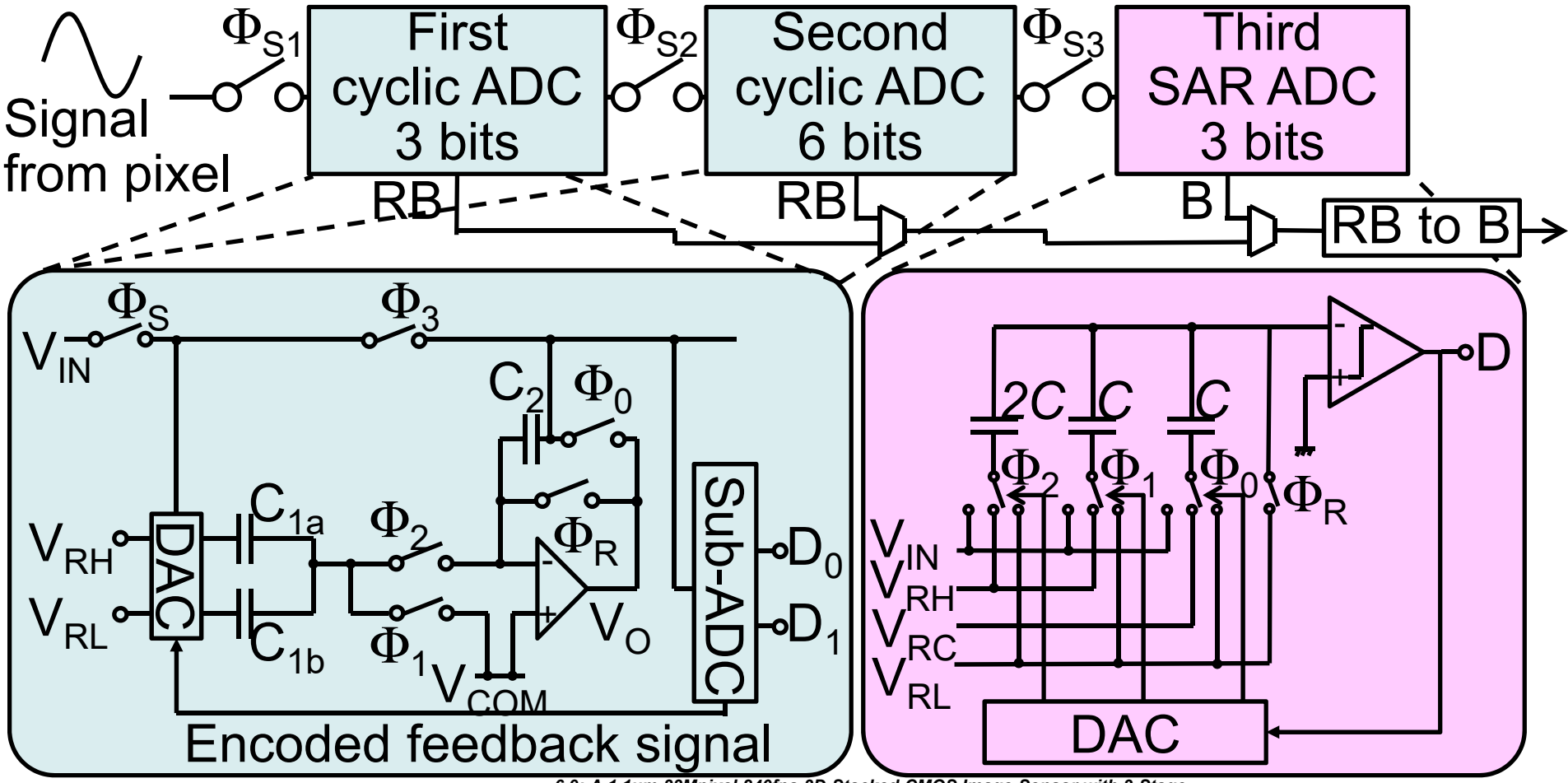
Architecture of the 12-bit cyclic-cyclic-SAR ADC

- The ADC is composed of a first single-ended cyclic ADC, a second single-ended cyclic ADC, and a third SAR ADC



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Reasons of ADC type selection

- A Cyclic ADC is suitable for pipelined operation and middle layout area
- A SAR ADC is suitable to save power consumption

Type	Cyclic	SAR
Pipelined operation	○	×
Area	△ (Middle layout area)	△ (Large numbers of bits are difficult)
Power consumption	△ (Needs amplifier)	○ (Without amplifier)
Stage	First and second	Third (Small layout area for 3 bits)

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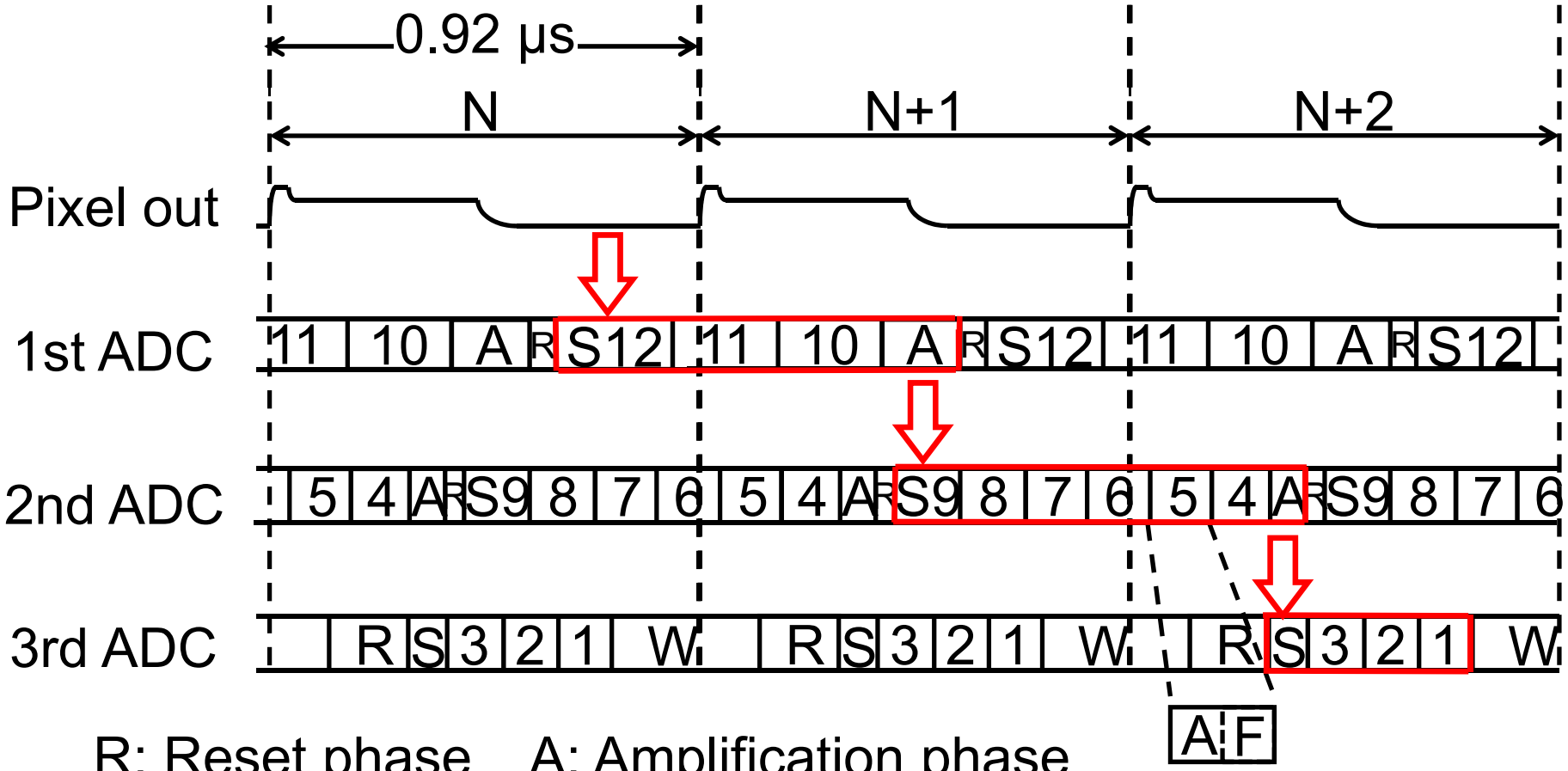
Timing diagram of pipelined operation

- 3-stage pipelined operation effectively reduces conversion time period to 0.92 µs



R: Reset phase A: Amplification phase

S: Sample phase F: Feedback phase W: Waiting phase

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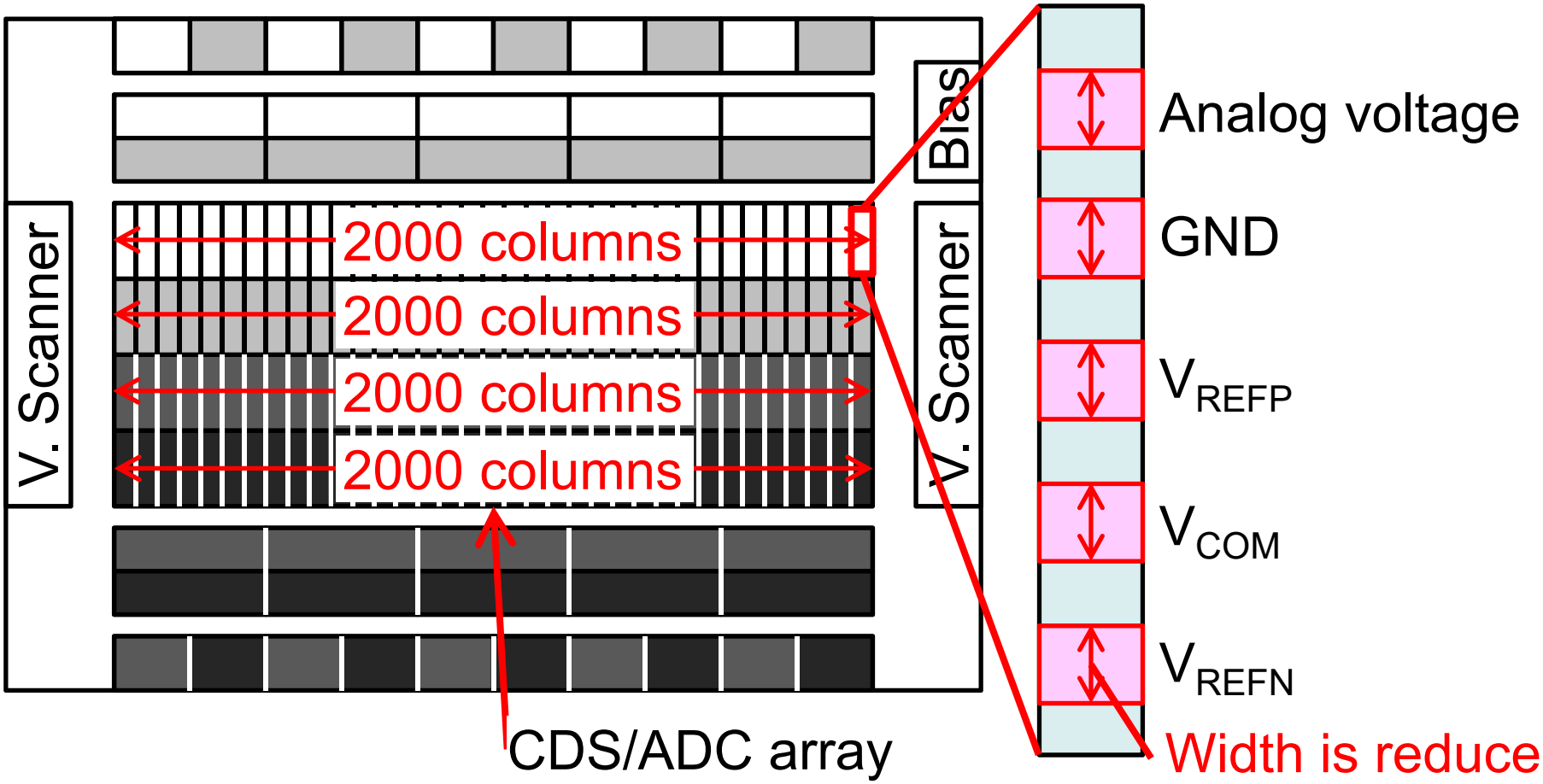
Layout area in cyclic ADC

- 3D-stack and interconnection technology enables to place an arrayed ADCs, and reduces layout area
- The width of the power supply wiring is reduced



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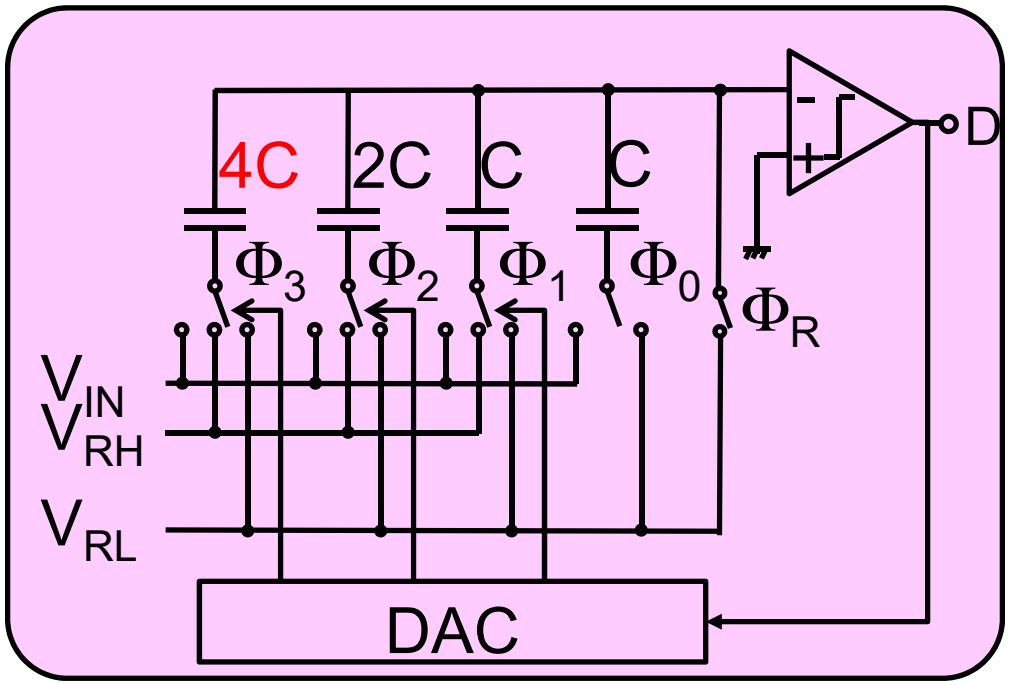
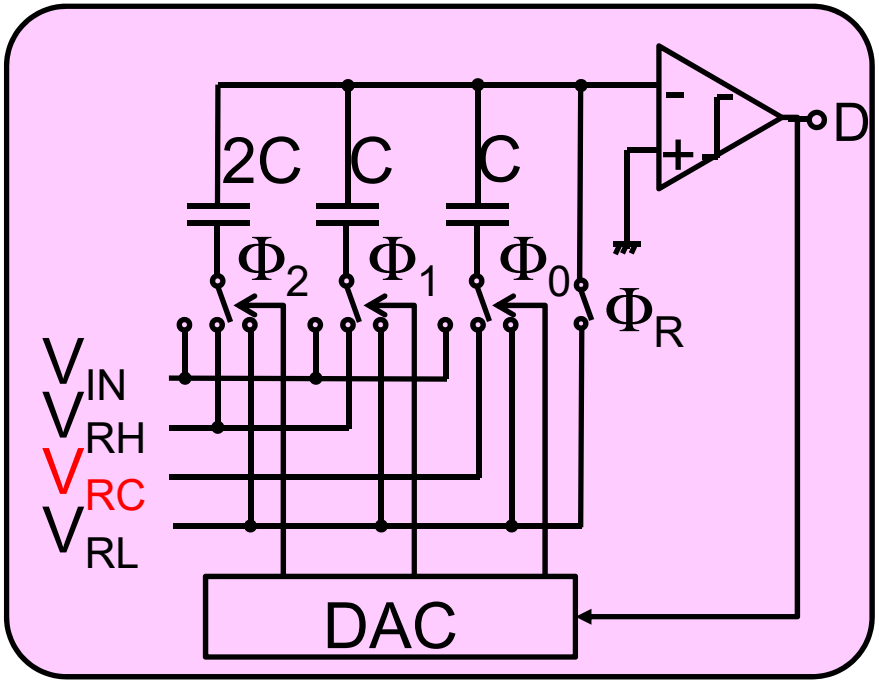
Reduction of layout area in SAR ADC

- Capacitor layout area of 4C is reduced by adding reference voltage V_{RC}



Conventional 3-bit SAR ADC



This 3-bit SAR ADC

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Design of ADC

- Half the conversion time period, smaller layout area, and almost the same power consumption

33Mpixel sensor	ISSCC (2012)	IISW (2015)	This work (2016)
Type	2-stage cyclic	2-stage cyclic	Cyclic-Cyclic-SAR
Resolution [bit]	12	14	12
Conversion time period [μs]	1.85	1.85	0.92 (High speed)
Size (W×L) [μm]	5.6×1730	6.4×1893	4.4×920
Area [μm^2]	9688	12115	4048 (Small area)
Power consumption [μW/ADC] (Simulation)	106	119	120 (Almost same)

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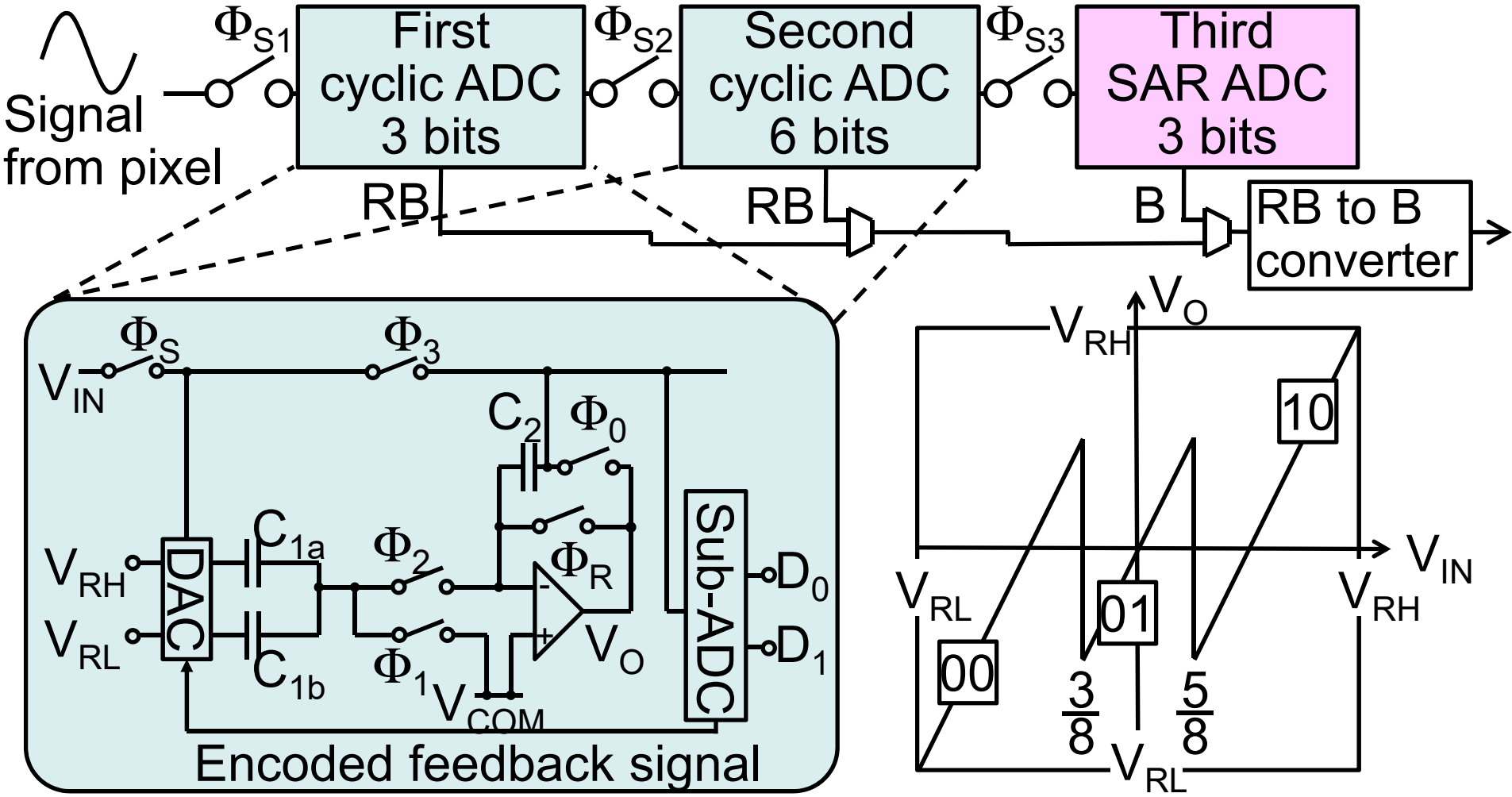
Redundancy of cyclic ADC

- The first and second cyclic ADCs output a 1.5-bit redundant binary code



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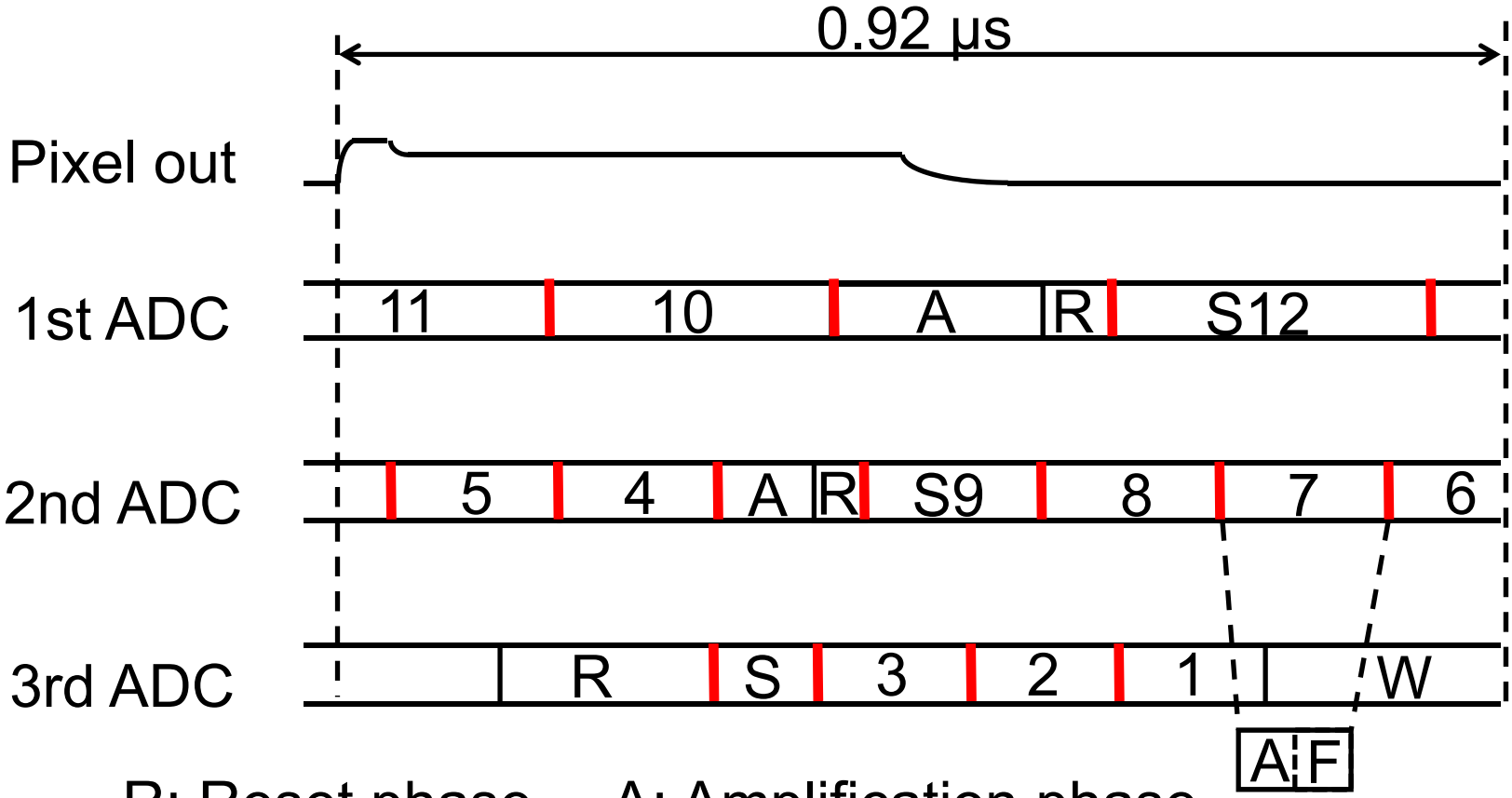
12-bit accuracy of pipelined operation

- A 12-bit accuracy is attained by preventing the interference from the clock timing



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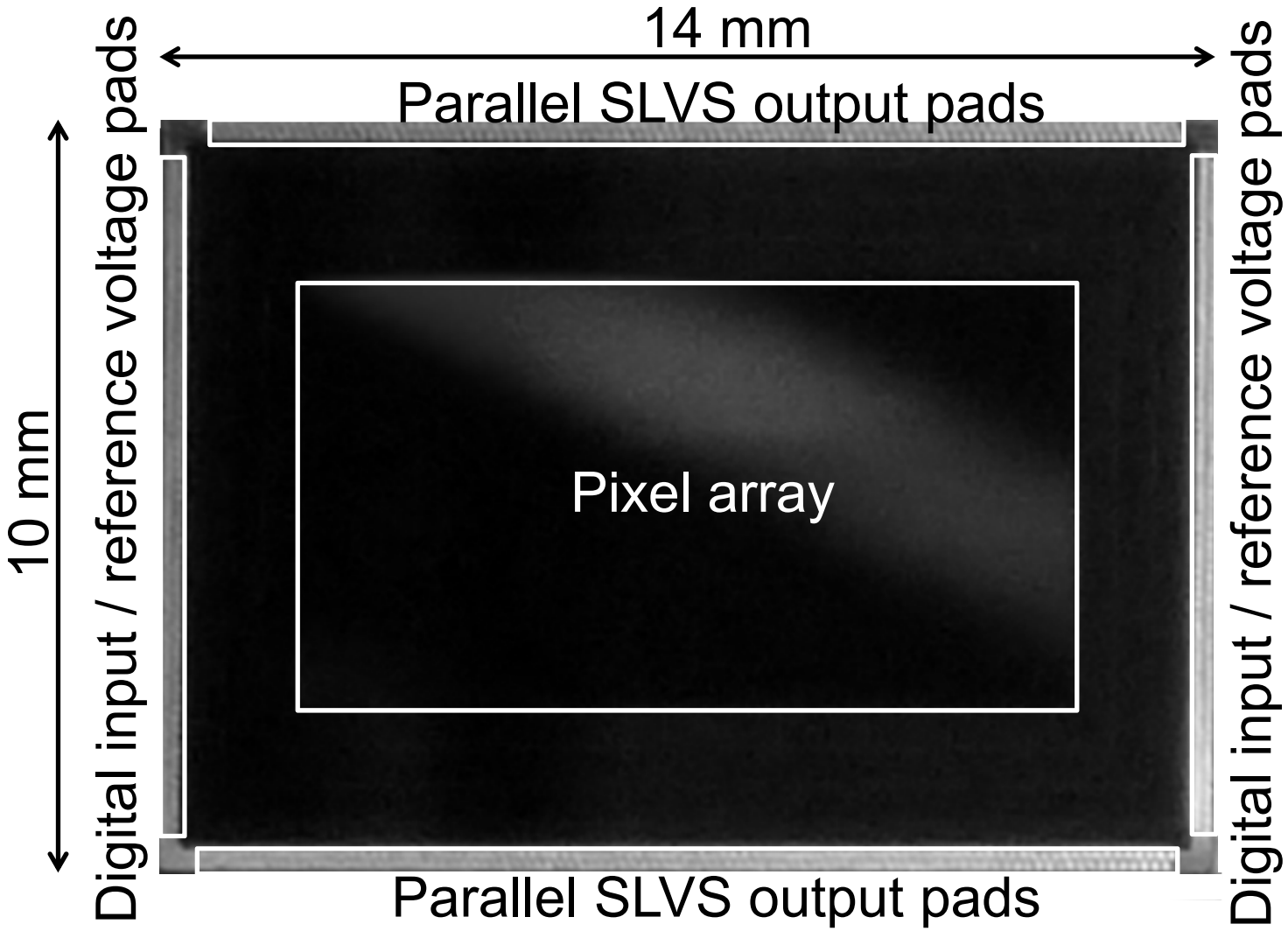
Die photograph

- The device is fabricated using a 3D interconnection process



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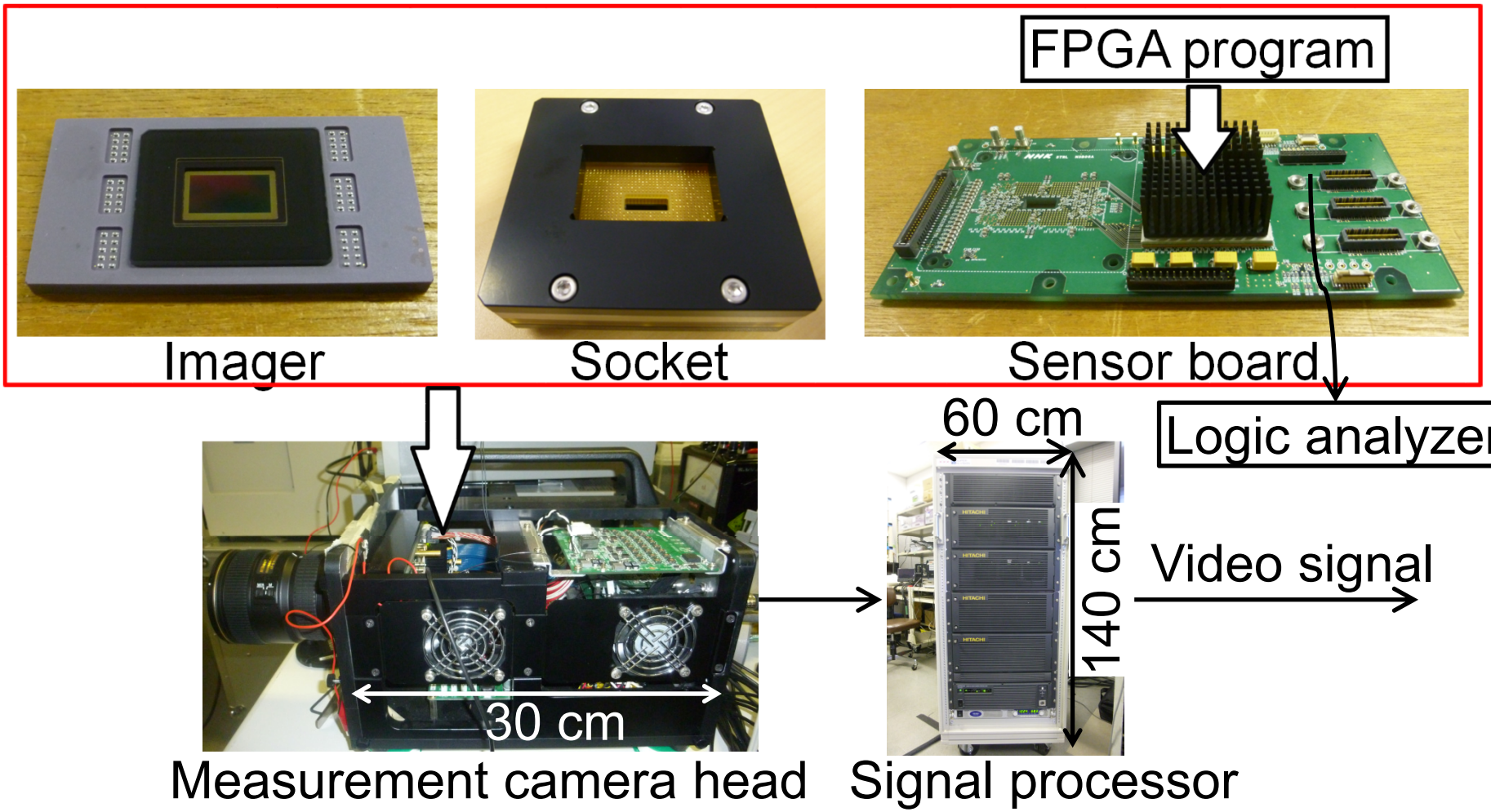
Measurement system

- The 33Mpixel image sensor is driven at 240 fps and all data is captured by FPGA



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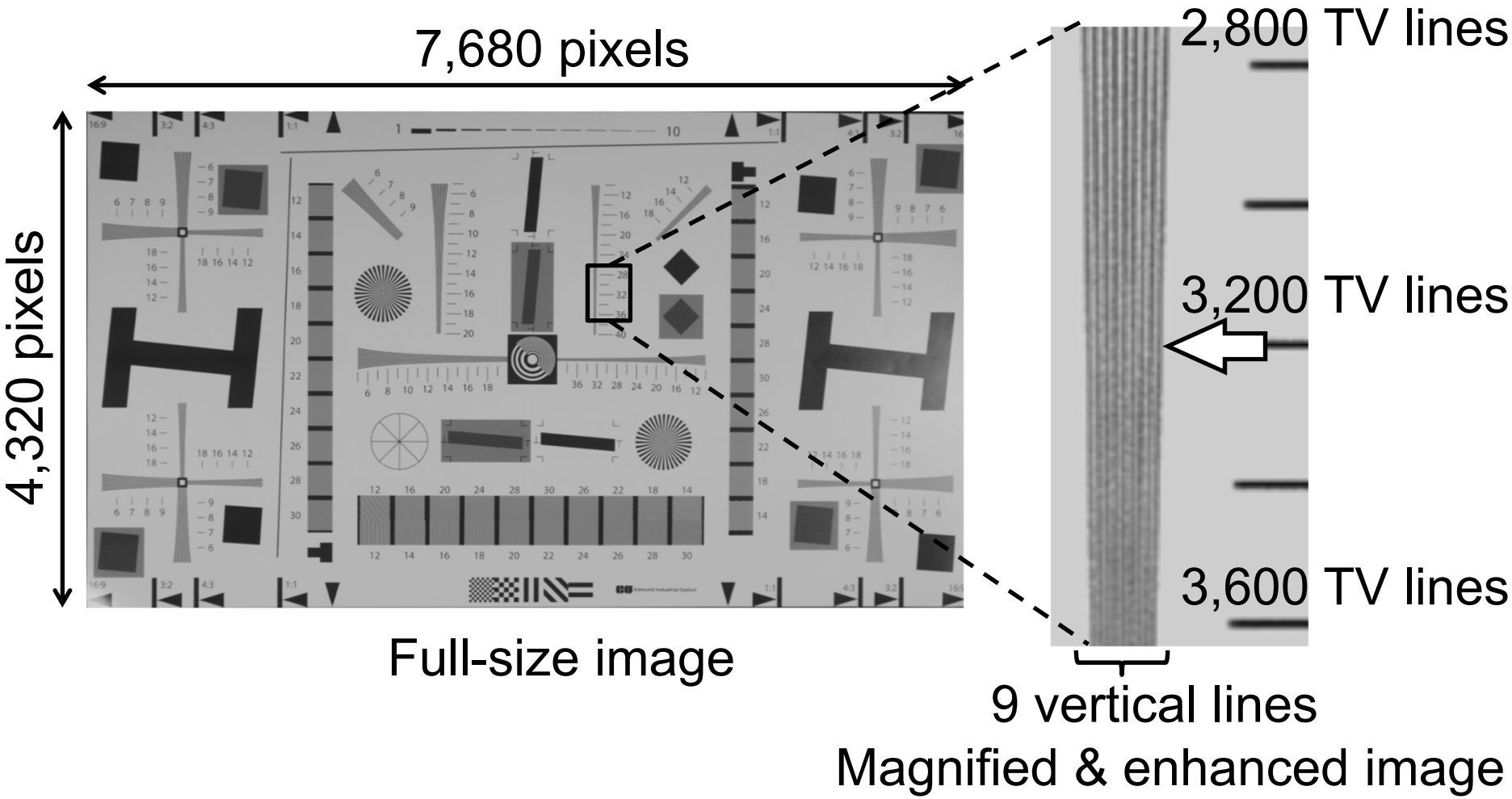
Reproduced full-size image

- 8K image is obtained at 240 fps
- Resolution is over 3,200 TV lines (lens iris: F4.0)



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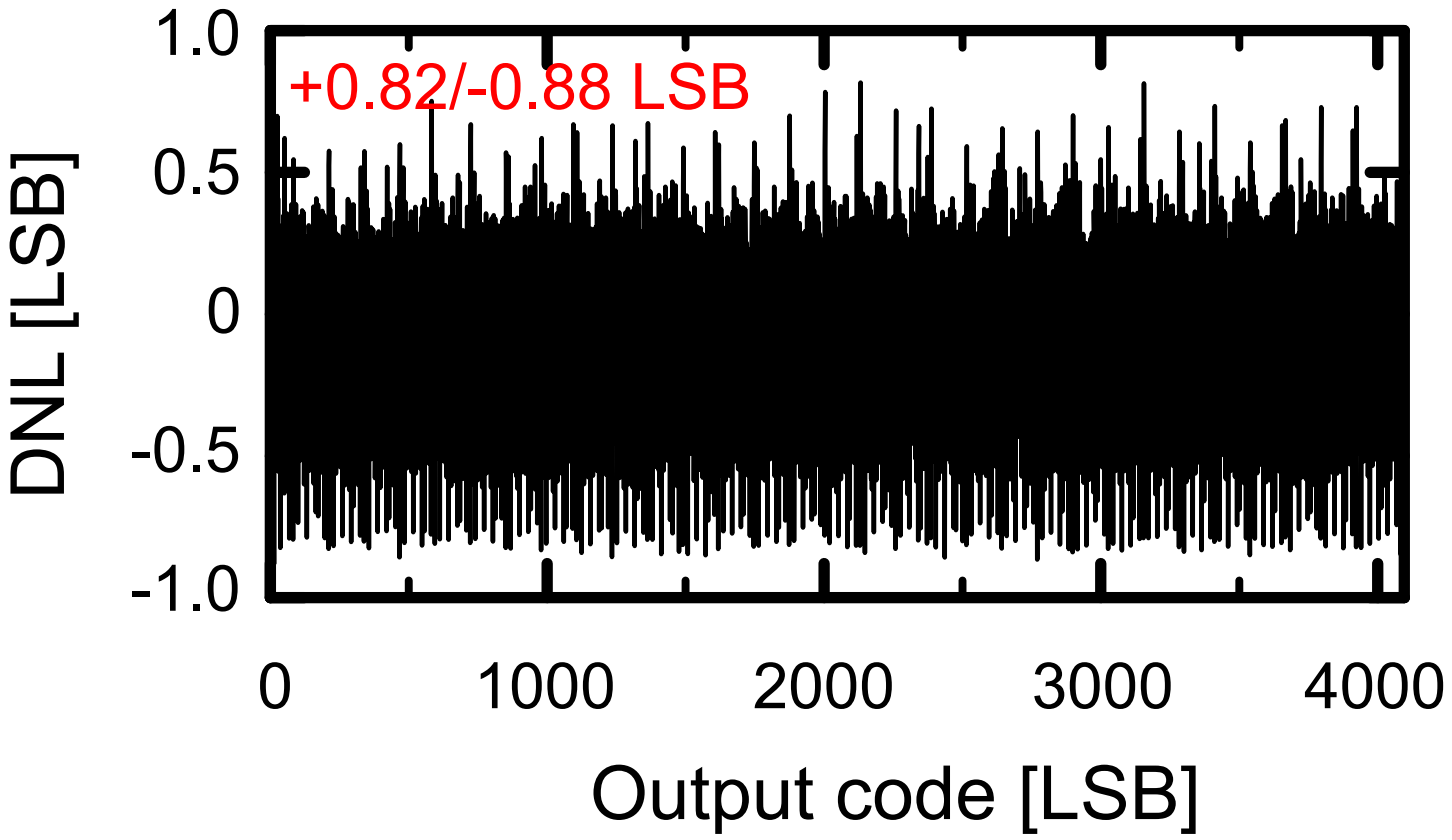
Measured DNL at 240 fps

- Differential nonlinearity (DNL) is within +0.82/-0.88 LSB
  - No missing code



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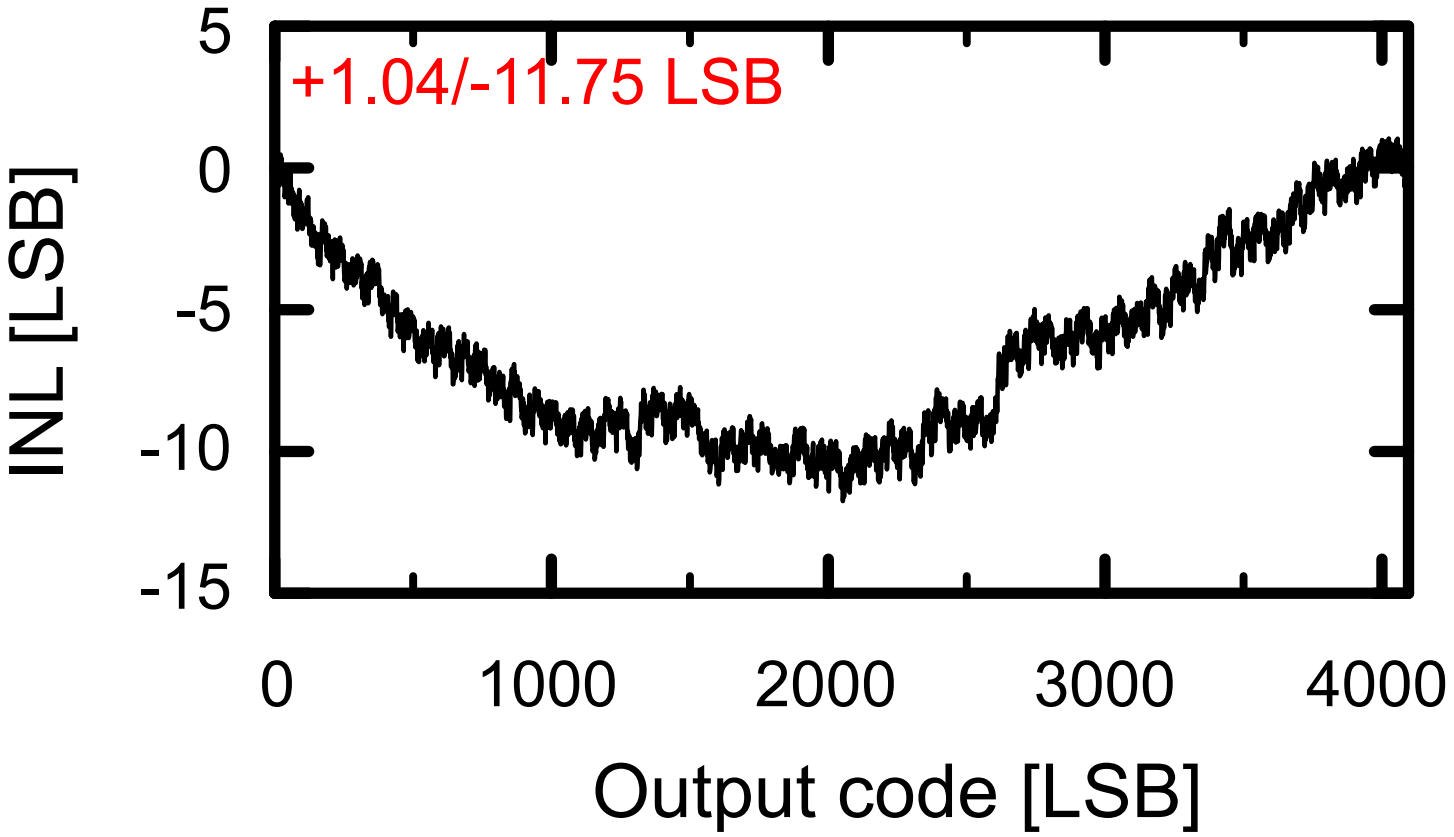
Measured INL at 240 fps

- Integral nonlinearity (INL) is within +1.04/-11.75 LSB
  - Variation is within 0.31% of 12-bit signal



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Summary of specifications (1/2)

Item	Value
Fabrication technology	45 nm 1P4M pixel 65 nm 1P5M logic
Supply voltage	1.2/2.5 V (digital), 2.5/2.8 V (analog)
Image size	8.448 mm (H)×4.752 mm (V)
Chip size	14 mm (H)×10 mm (V)
Number of effective pixels	7,728 (H)×4,368 (V) (33M)
Pixel size	1.1 μm×1.1 μm (2×2-shared pixel)
Frame rate	240 fps (maximum)
Conversion time period	0.92 μs
ADC resolution	12 bit

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Summary of specifications (2/2)

Item	Value
ADC DNL	+0.82/-0.88 LSB
ADC INL	+1.04/-11.75 LSB
Conversion gain	92 μV/e-
Sensitivity	0.55 V/lx-s (w/o ML & CF, CIE A-light, IR cut filter)
Full well capacity	5,700 e-
Random noise	4.5 e-rms (gain: 1.0) at 240 fps 3.6 e-rms (gain: 4.0) at 240 fps
PRNU	<1.3% (Dead-line free)
Power consumption	3.0 W at 240 fps

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Definition of FoM1 and FoM2

- $$FoM_1 = \frac{Power \cdot N_{NOISE}}{f_p} \times 10^9 \quad [e^- \cdot nJ]$$

FoM1: Noise and Power Performance per Pixel Rate

- $$FoM_2 = \frac{Power \cdot N_{NOISE} \cdot Gain}{f_p \cdot 2^N} \times 10^{12} \quad [e^- \cdot pJ/step]$$

FoM2: Power Performance per Dynamic Range and Pixel Rate

f_p = Pixel rate (No. of pixels × frame rate)

N = bit resolution

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Performance comparison

Item	[3]	[1]	[5]	[6]	IISW	This work
Year	2011	2012	2015	2015	2015	2016
ADC type	SS	2-stage cyclic	SS	SAR	2-stage cyclic	Cyclic-Cyclic-SAR
ADC resolution [bit]	12	12	12	12	14	12
Frame rate [fps]	120	120	30	60	120	240
No. of pixels [Mpixel]	17.7	33	20	133	33	33
Conversion gain [μV/e-]	—	—	76.6	80	61	92
Random noise [e-rms]	2.75	3.0	1.3	7.68	5.2	3.6
Gain	11.2	7.5	22.4	2	3.5	4.0
Power consumption [W]	3	2. 67	0.532	11	3.2	3.0
Pixel rate [Gpixel/s]	2.12	3.98	0.62	7.96	3.98	7.96
FoM1 [e- · nJ]	3.89	2.01	1.11	10.61	4.18	1.36
FoM2 [e- · pJ/step]	10.6	3.68	6.10	5.18	0.89	1.32

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Summary

- A 1.1μm 33Mpixel 240fps BSI 3D-stacked CMOS image sensor with a 12-bit 3-stage cyclic-based ADC has been developed.

- The ADC architecture and the interconnection technology achieve a high frame rate of 240 fps in 33 Mpixels for the first time.

- Random noise of 3.6 e- and low power consumption of 3.0 W are attained at high pixel rate of 7.96 Gpixel/sec.

- Acknowledgements:
The authors would like to thank the members of the TSMC CIS Team for their support of this work

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